

MS-7A38 Ver:8.1

CPU:
amd am4
System Chipset:
Promontory B450
(Value DIY or System Builder)

Main Memory:
DDR IV * 4 MAX:64 GB

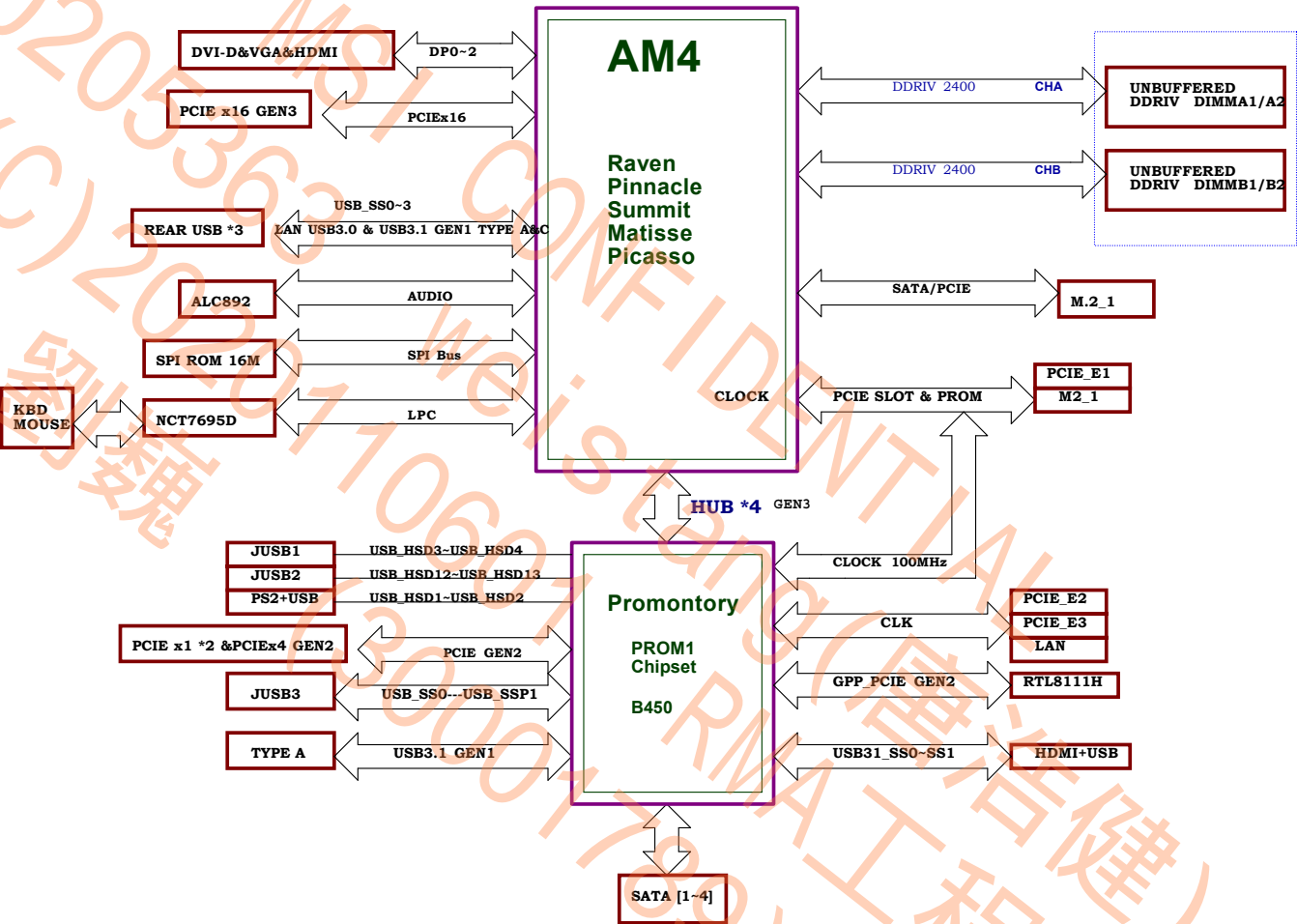
VRM
RT8894 4+2

On Board Chipset:
LPC Super I/O --NCT6795D
LAN RTL8111H
Azalia CODEC - Realtek ALC897

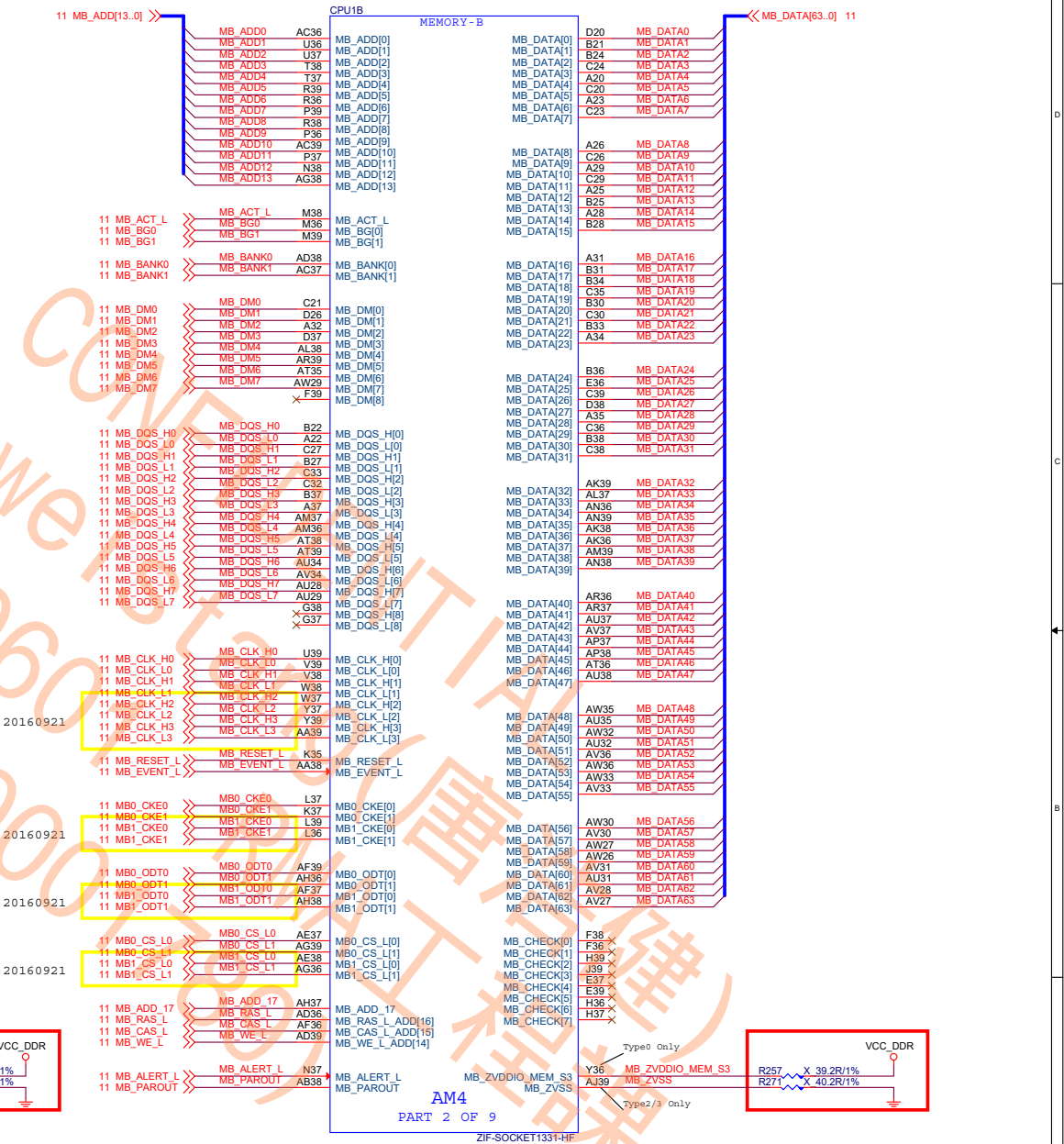
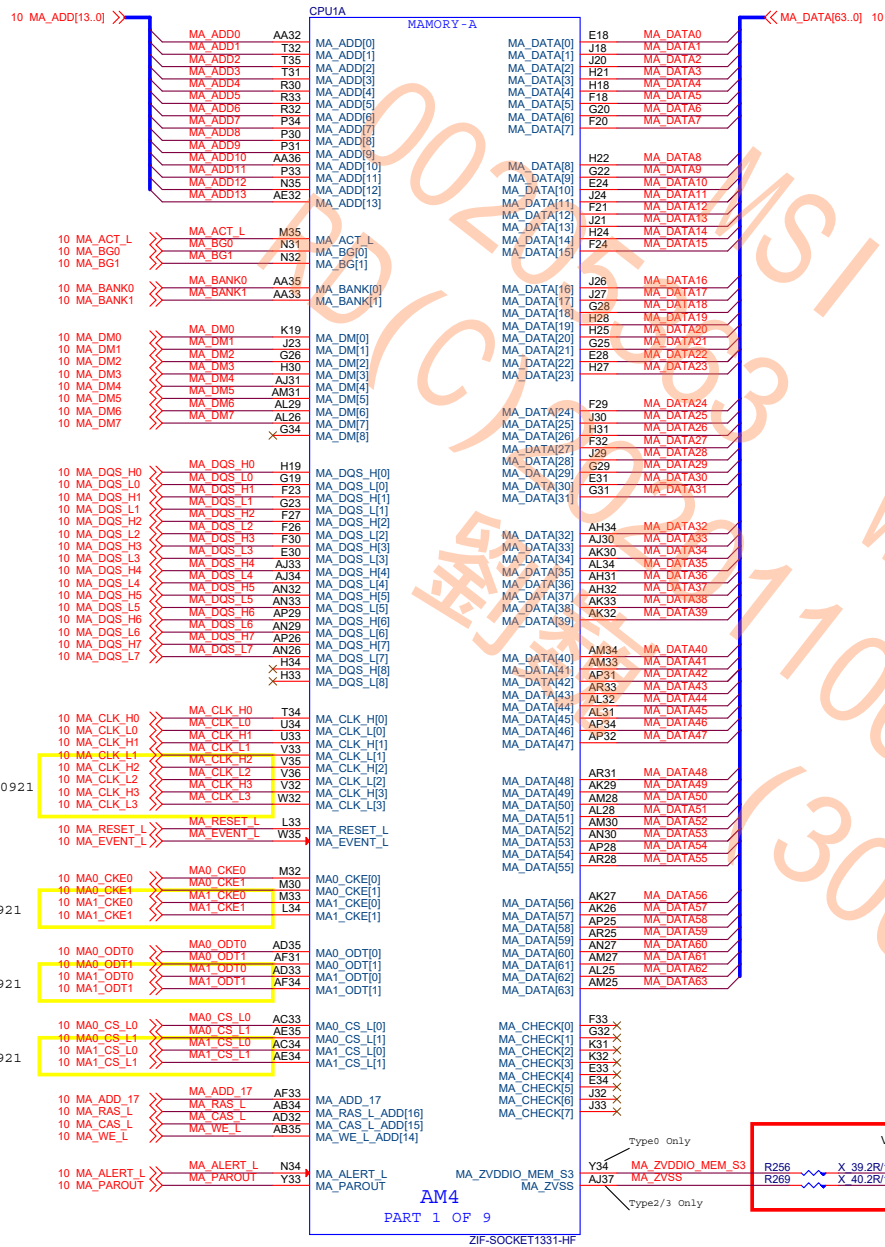
Expansion Slots:
From CPU
PCI Express X16 Slot * 1
PCI Express X1 Slot * 1
PCI Express X1 Slot * 1

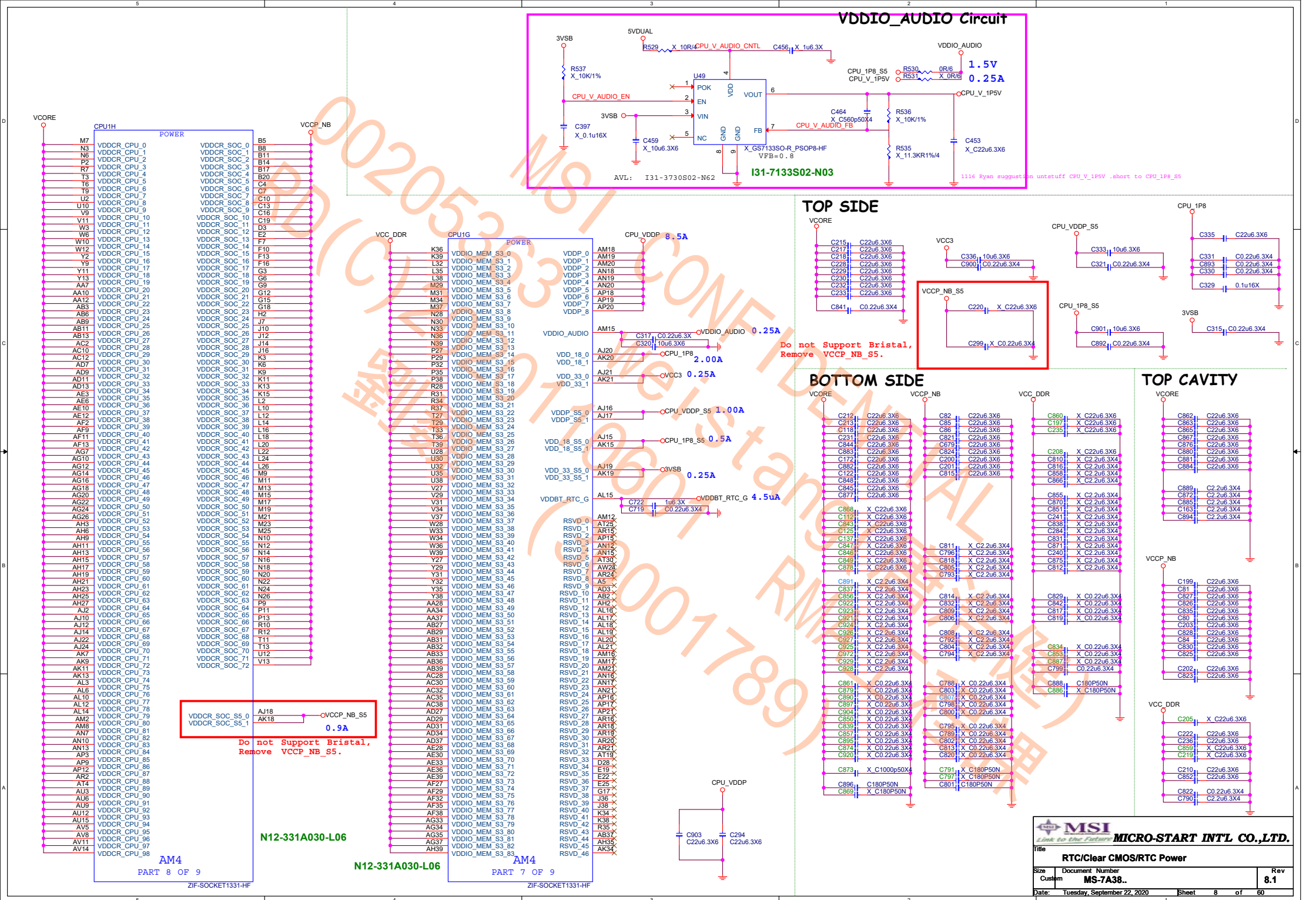
OCF IC:
RT9553

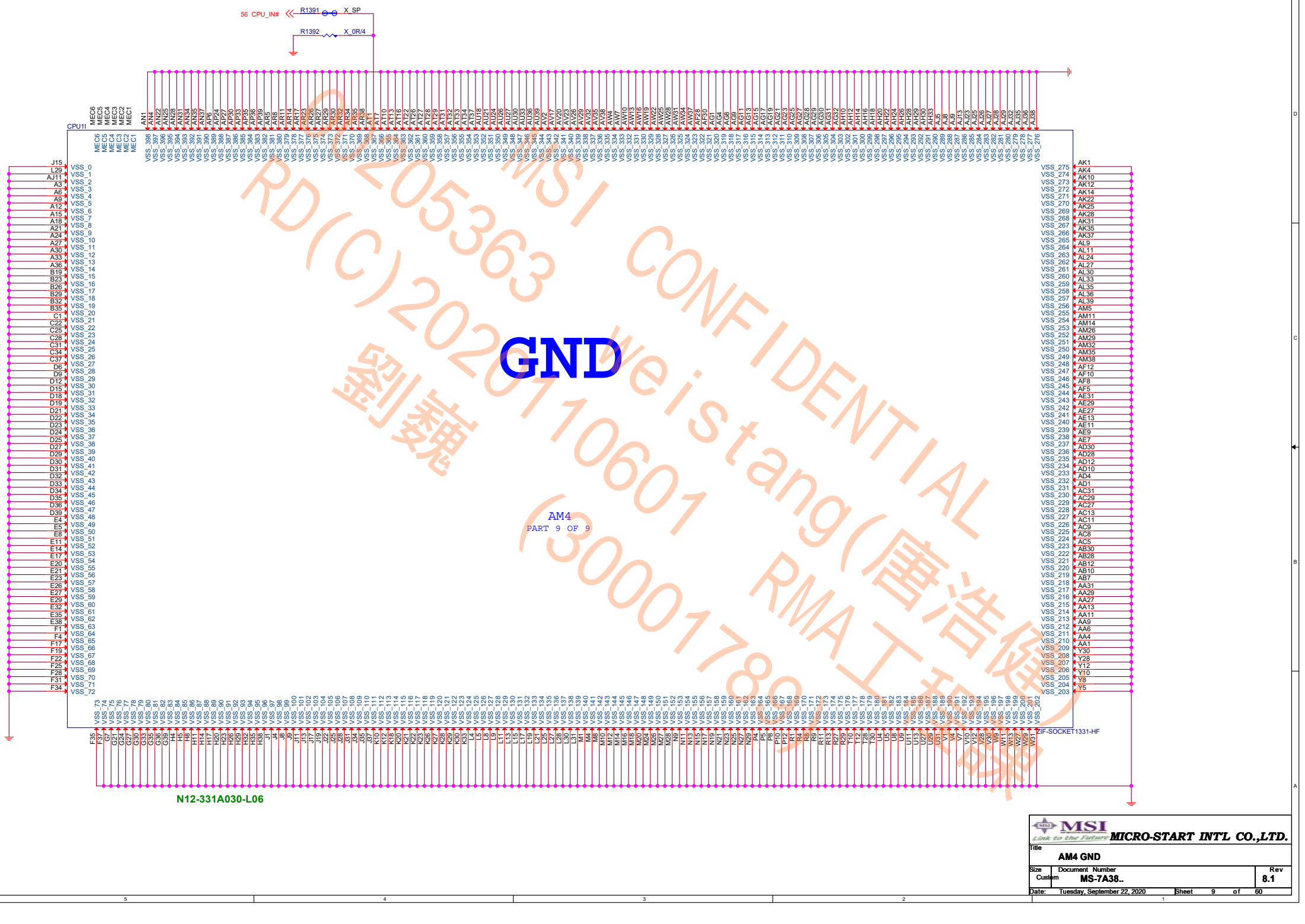
FUSION BLOCK DIAGRAM



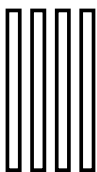
01 Block Diagram	37 DVI Connector
02 Cover Sheet	38 HDMI
03 FM4 DDR4 I/F	39 ACPI uPI-5VDIMM&3VSB
04 AM4 PCIE/SATAE	40 PM-NB681-1.05V/GS7133-2.5V
05 AM4 Display/Audio	41 DDR PWR VPP25/VTT-MP2329G
06 AM4 SVI/ACPI/GPIO	42 DDR4 8125E Power
07 AM4 LPC/SPI/USB/CLK/STRAP	43 CPU Power 1P8V-MP2329C
08 AM4 Power/RTC Power/ 09 AM4 GND	44 CPU Power VDDP-RT8125E
10,11 DDR4-DIMM CH-A/B	45 CPU Power Connector/PWRGD
12,13 DDR4-POWER/GND	46 CPU Power RT8894 4+2 Phase
14 Promontory-PCIE/SATA/SATAE	47 / 48 CPU Power Phase 1-4
15 Promontory-USB/OC	49 CPU Power NB Phase 1-2
16 Promontory-CLK/ACPI/GPIO	50 CPU Power NB Switch/NCT3933
17 Promontory-Power / 18 Promontory-GND	51 RT9553 CURRENT SENSE
19 Reserve	52 ATX/Front Panel
20 PCIE X16 /21 PCIE X1*2) SLOT	53 ALL LED
22 SIO NCT6795	54 ALL LED Control
23 HWM/COM/Debug LED	55 BOM Option
24 CPU/SYS FAN Control TYPE K	56 RTC Circuit/Moat Cap
25 CPU/SYS FAN 2	57 History
26 LAN-RTL8111H	58 Power Sequence
27 / 28 Audio ALC892	59 GPIO MAP
29 USB Rear PS2+USB2.0	60 Power Map
30 USB Rear LAN+USB3.1 GEN1	
31 Rear USB3.1 TYPE A	
32 USB Rear HDMI+TYPE A	
33 USB Front Side	
34 M.2	
35 SATA Connector	
36 DP to VGA ITE6516	







A1 A2 B1 B2



N13-2880561-L06

SCLK0 SCLK0
SDATA0 SDATA0

R427 X SP
R431 X SP

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMA1	A4
DIMMB0	A2
DIMMB1	A6

VCC_DDR

R266

1KR4

MA_RESET_L

MA_EVENT_L

MA_ALERT_L

MA_ACT_L

MA_PAROUT

SAVE_N_NC

RFU-0

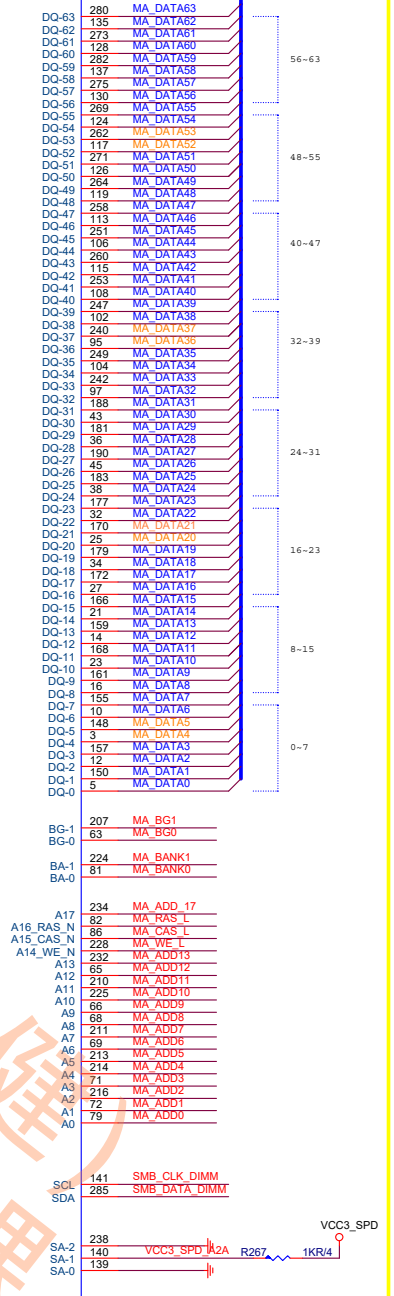
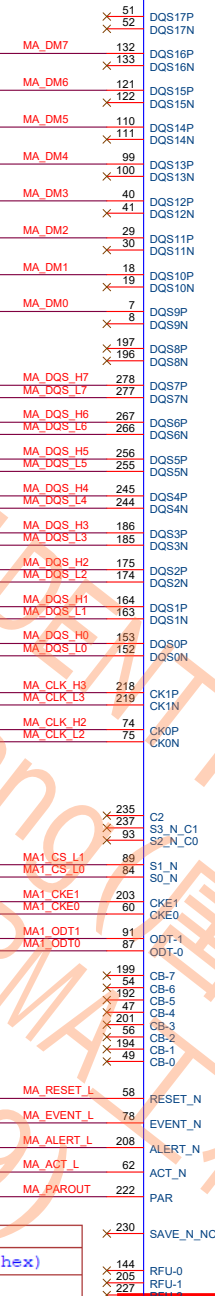
RFU-1

RFU-2

DDRIV-288P_BLACK-RH-21

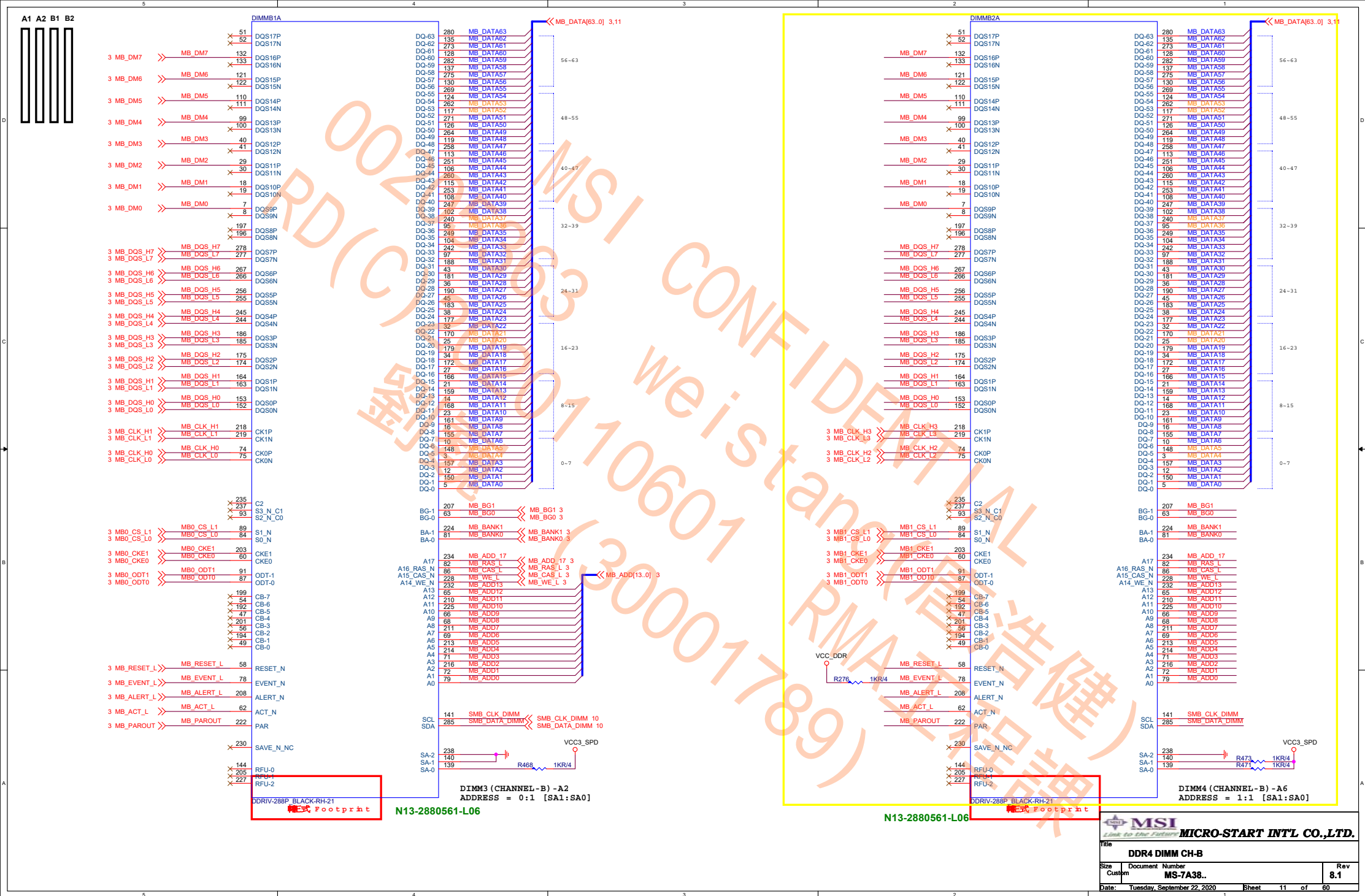
Footprint

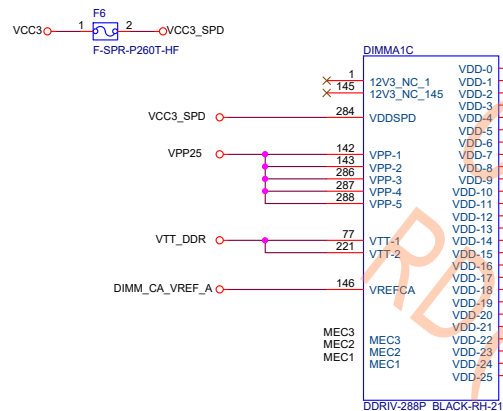
N13-2880561-L06



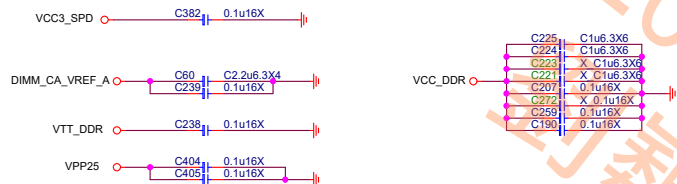
MSI MICRO-START INTL CO.,LTD.

Title		Rev	
DDR4 DIMM CH-A		8.1	
Size		Document Number	
Custom		MS-7A38..	
Date:		Tuesday, September 22, 2020	
Sheet		10 of 60	



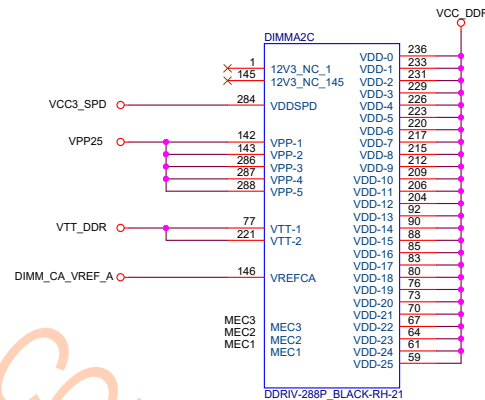


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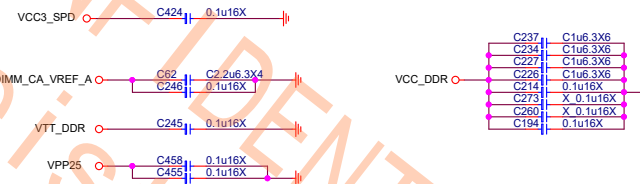


N13-2880561-L06

DIMM SLOT PN BY SPEC



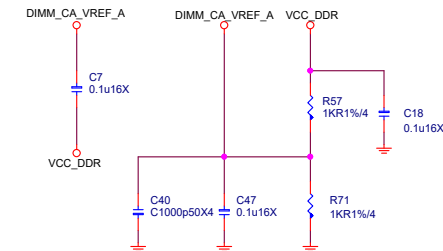
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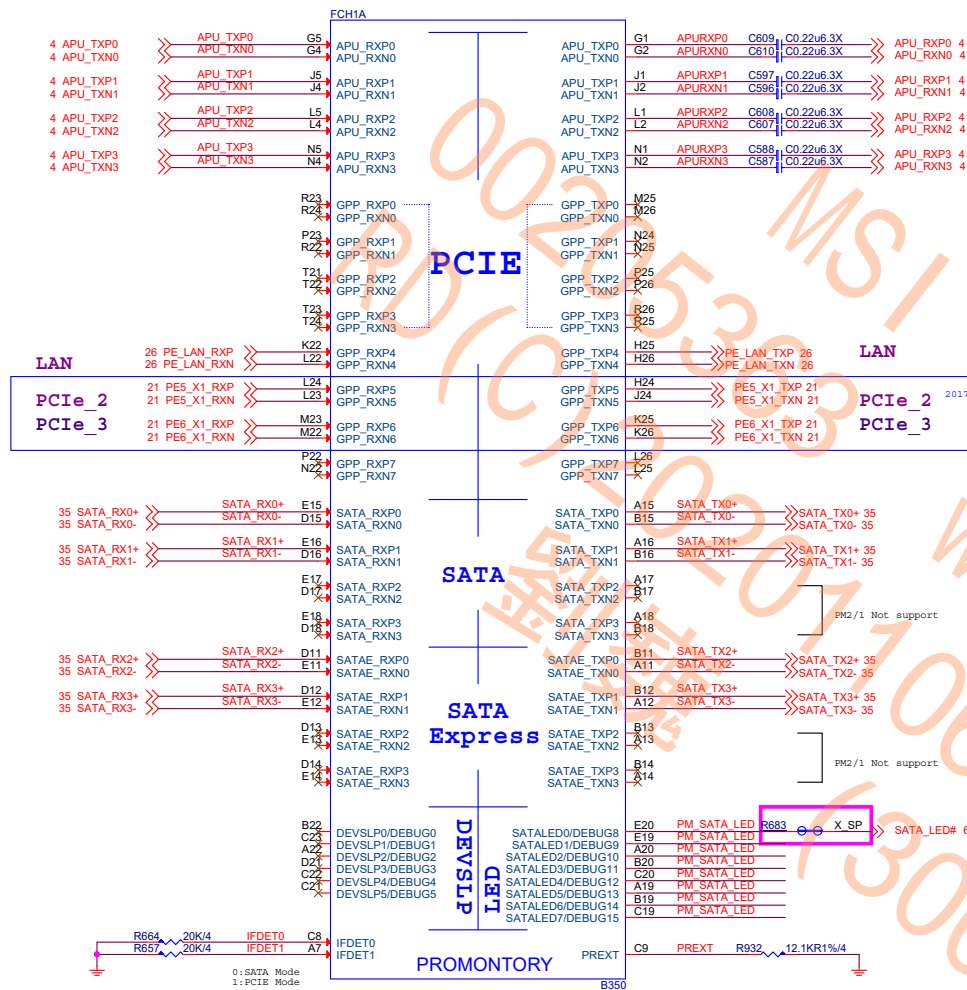


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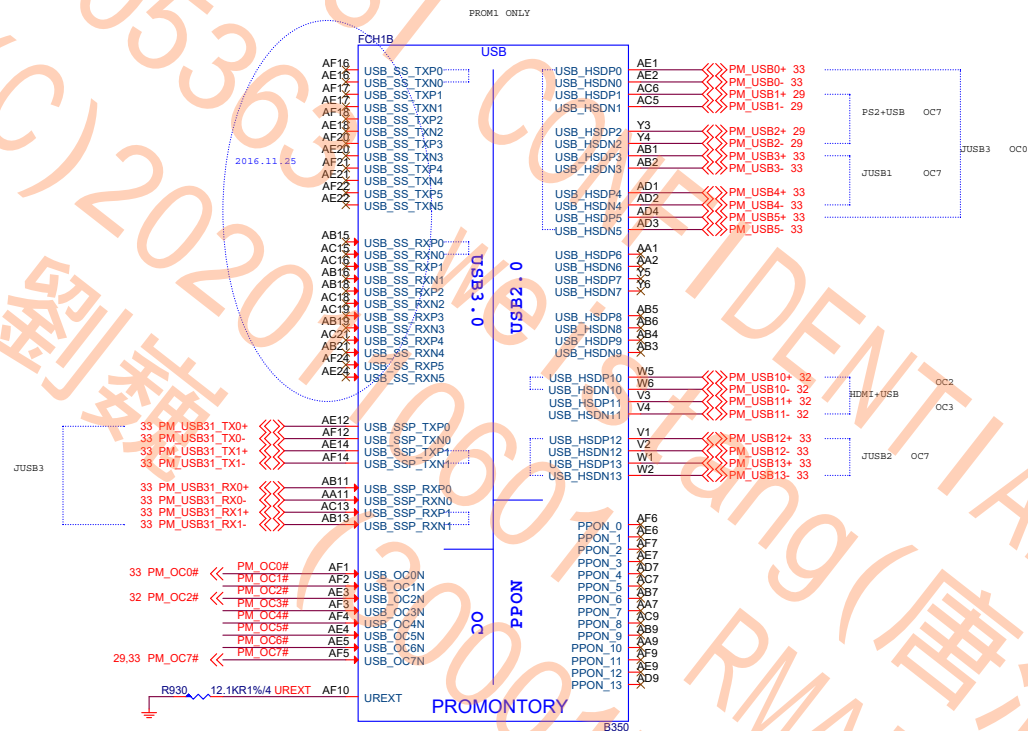
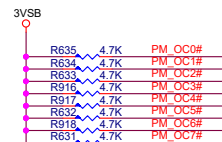
DDR VREF

(place resistors close to DIMMs)

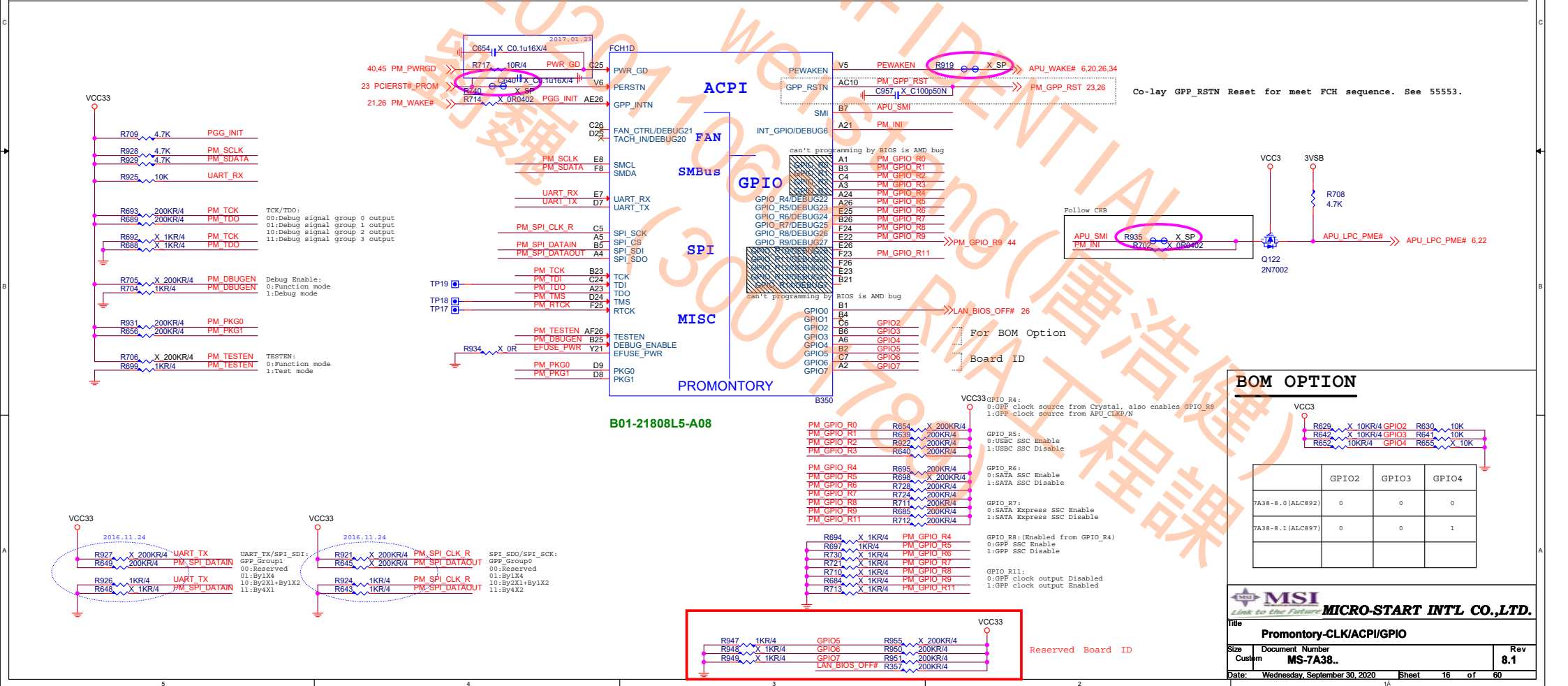
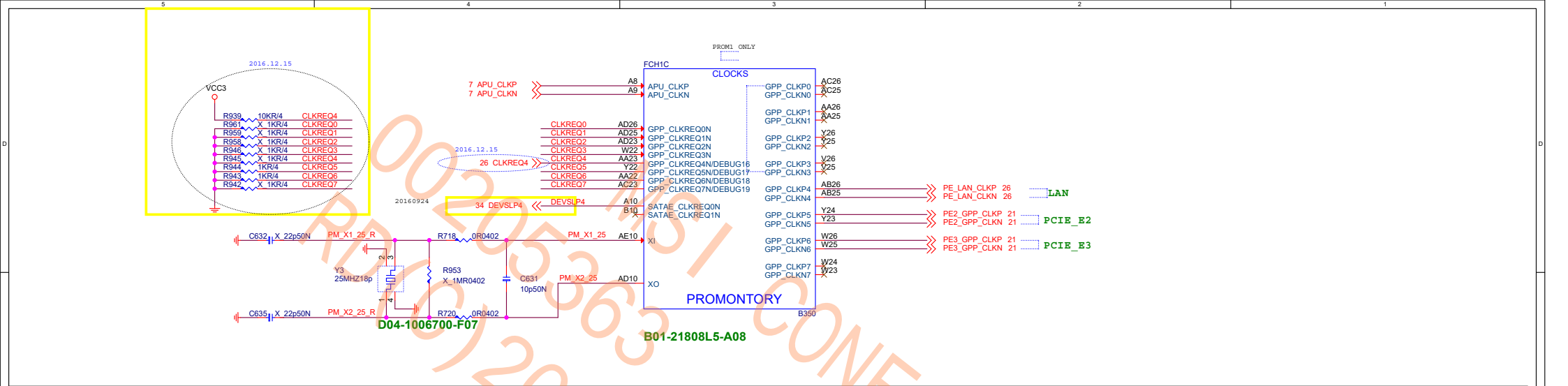


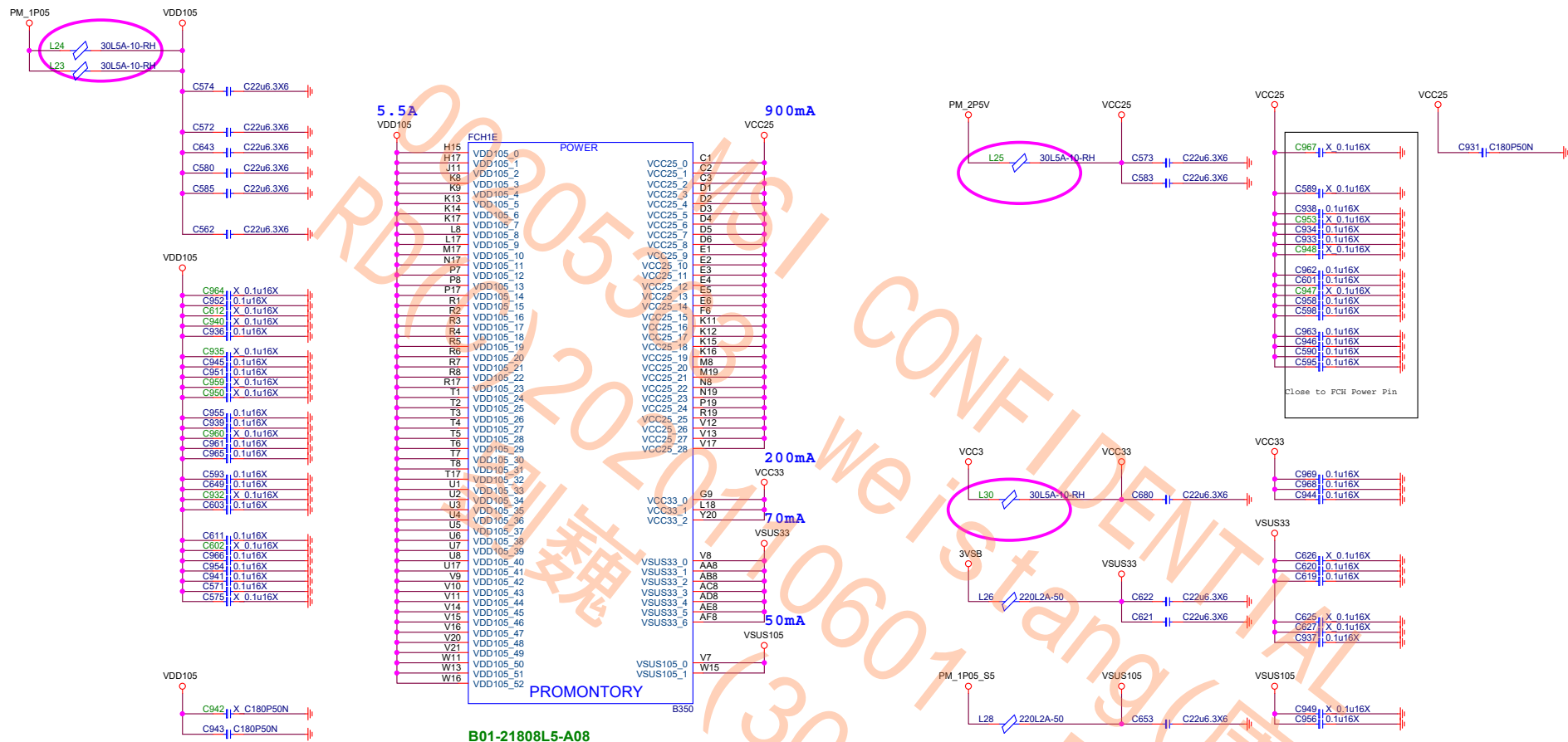


B01-21808L5-A08




B01-21808L5-A08





MSI CONFIDENTIAL
00205363
RD(C)2020110601
劉魏
weistang(唐浩健)
(30001789)
RMA工程課

 MICRO-START INTL CO.,LTD.		
Title PCIE CLK		
Size	Document Number	Rev
Custom	MS-7A38..	8.1
Date:	Tuesday, September 22, 2020	Sheet 19 of 60

PCI EXPRESS x16 Slot

PCIEX1 12V 0.5A
3.3V weak 375mA

C71-27118A1-F70

C71-56106P1-F70

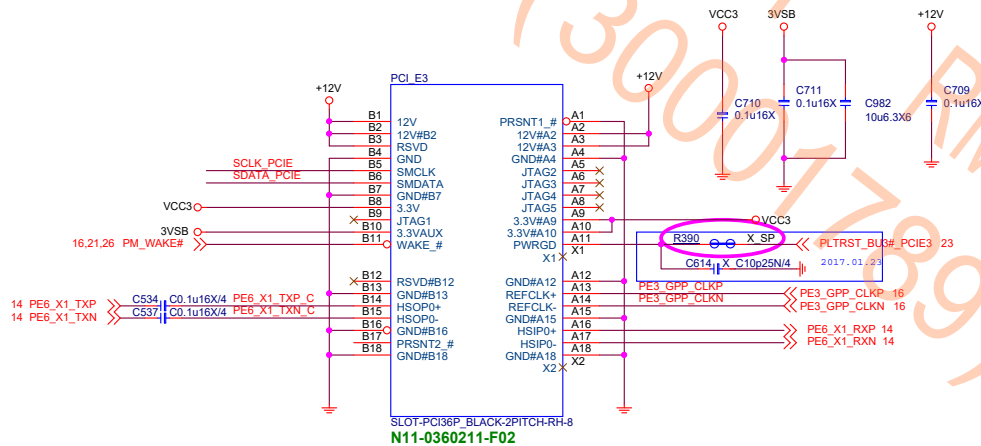
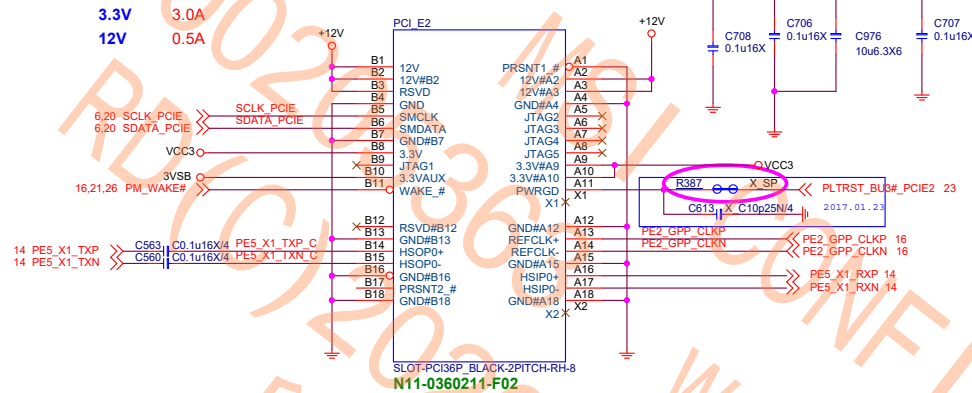
SMBus separate circuit

SMB SEL
GPIO Default High

D0G-05A0529-A68

N11-1641811-L06

PCIEX1 12V 0.5A
3.3V weak 375mA

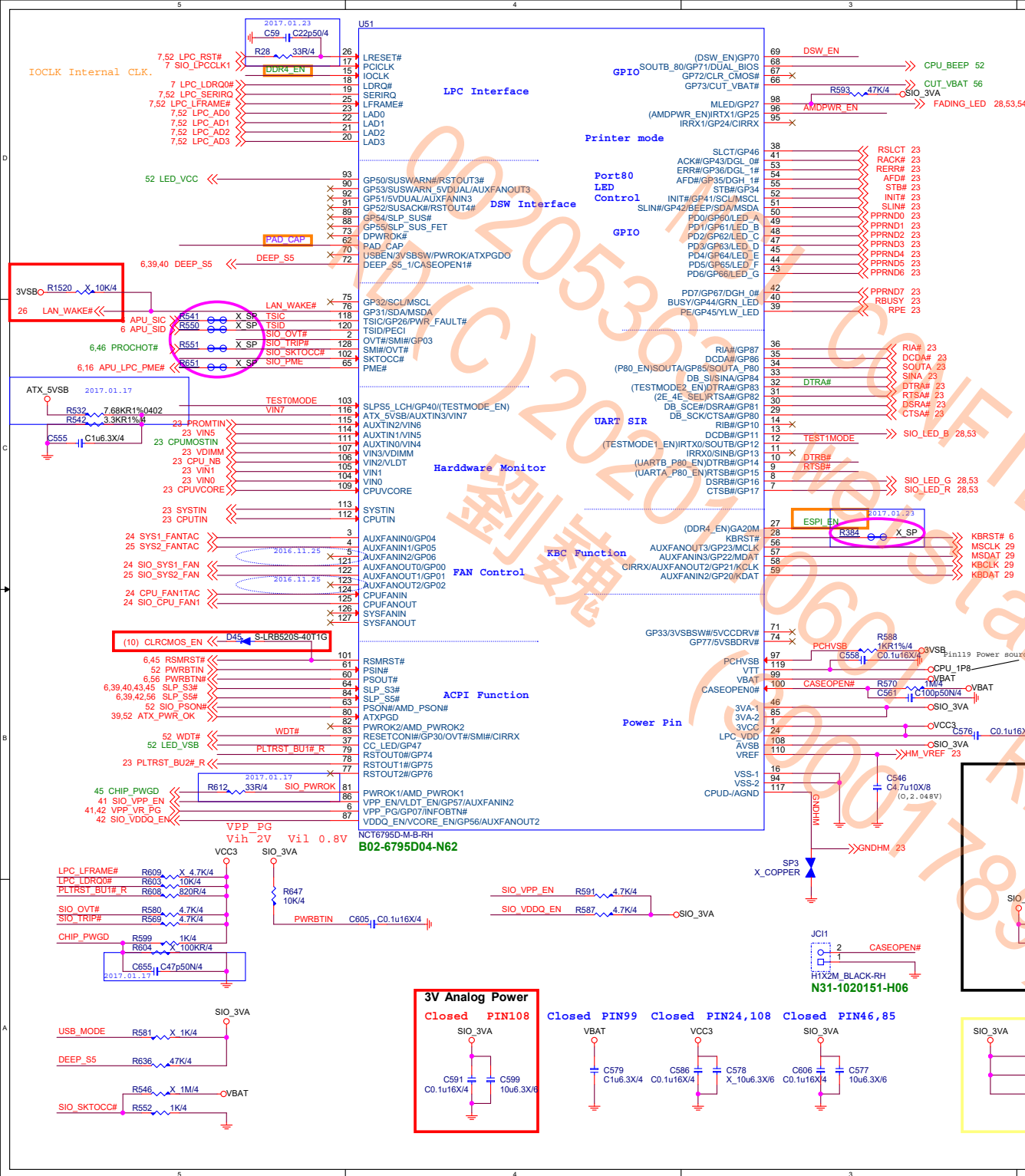


PCI Express x1 Slot *2

+12V	- 1 A
+VCC3	- 6A
+3V3_S5 (wake)	- 750mA
+3V3_S5 (no wake)	- 40mA

MSI
Link to the Future
MICRO-START INTL CO.,LTD.

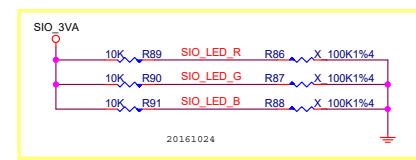
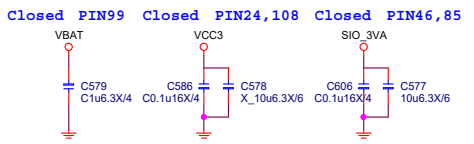
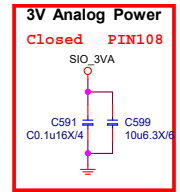
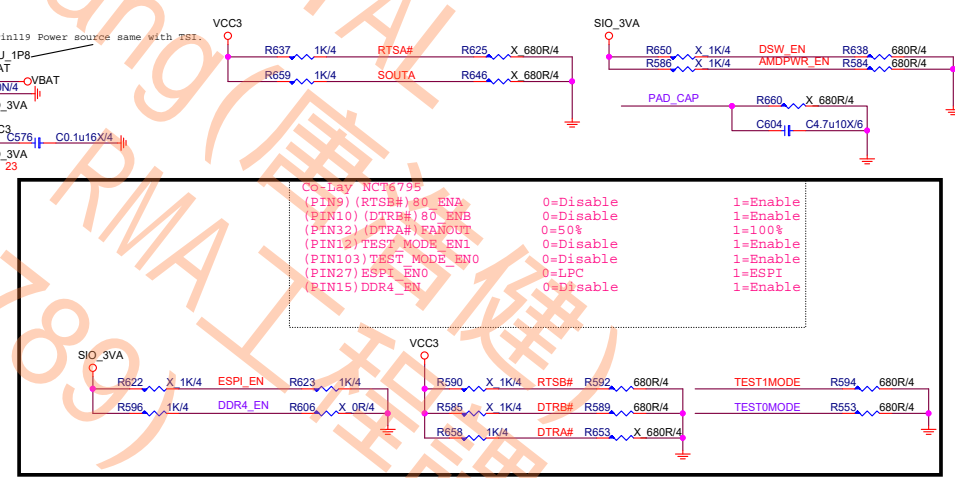
Title PCIE X4(X1*2) SLOT		
Size Custom	Document Number MS-7A38..	Rev 8.1
Date: Tuesday, September 22, 2020	Sheet 21	of 60



POWER ON STRAPPING PIN FOR NCT6793/6795

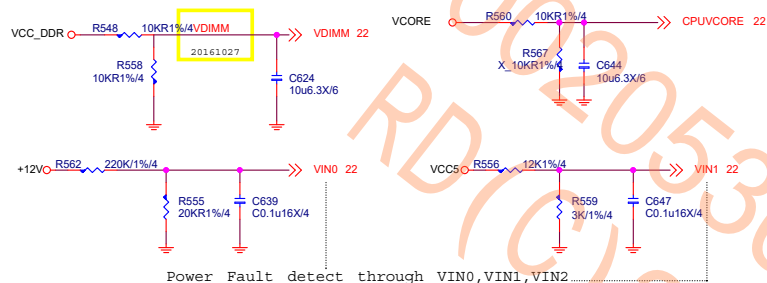
PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESP1_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low, BIOS must programming LPT or GPIO



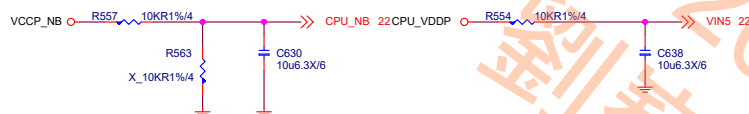
HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect

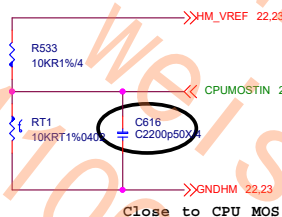
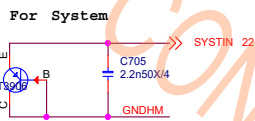
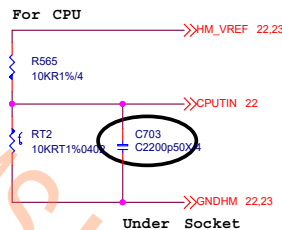


Power Fault detect through VIN0, VIN1, VIN2

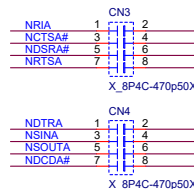
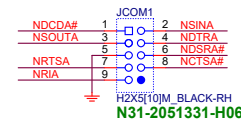
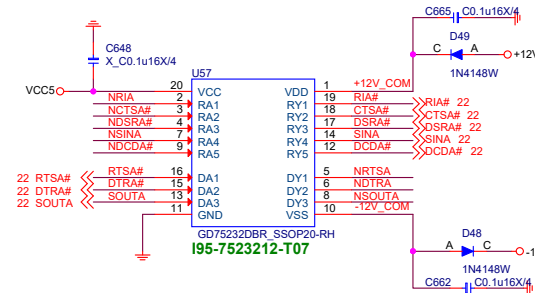
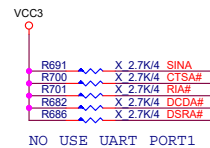
Inform BIOS disable VIN2 with Power Fault



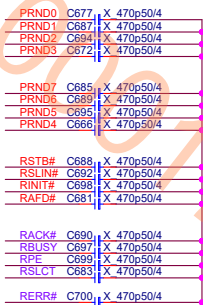
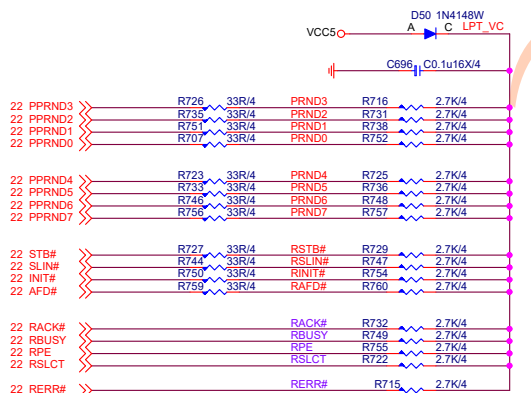
TEMP SENSOR



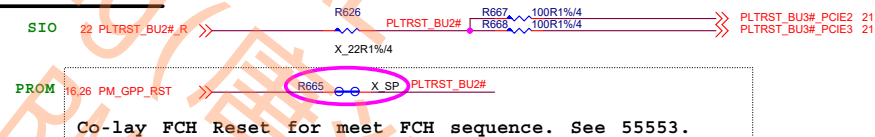
COM PORT



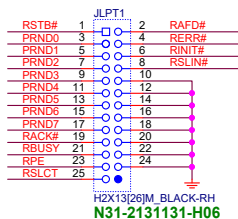
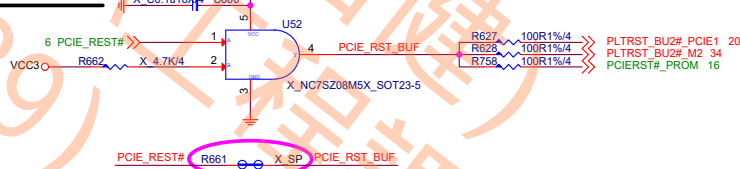
PARALLAL PORT



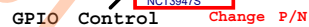
PROM RESET



CPU RESET



2. GPIO 模式切換 PW M/DC M O D E



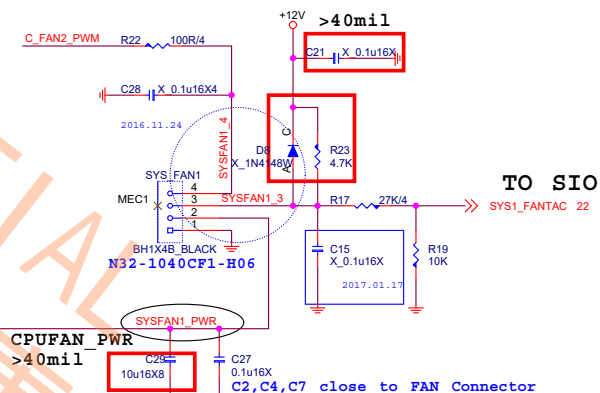
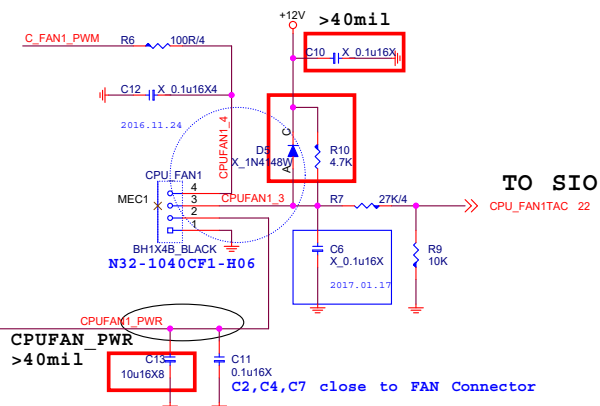
	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

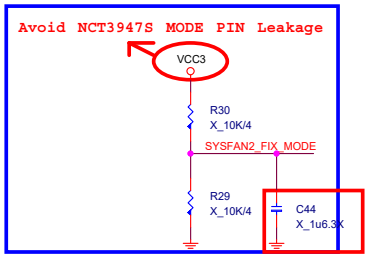
Internall pull up 1.65V



	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

Internall pull up 1.65V

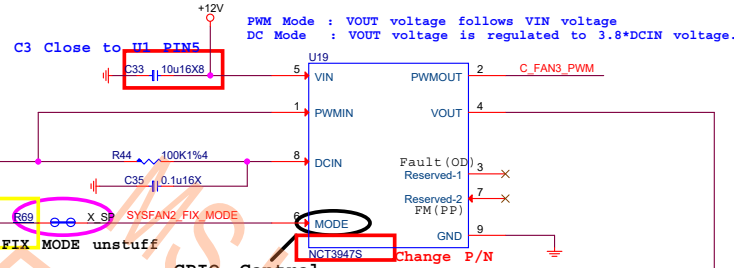




Resever For FIX DC or PWM MODE USE By PM SPEC

From SIO

22 SIO_SYS2_FAN
6 SYSFAN2_MODE

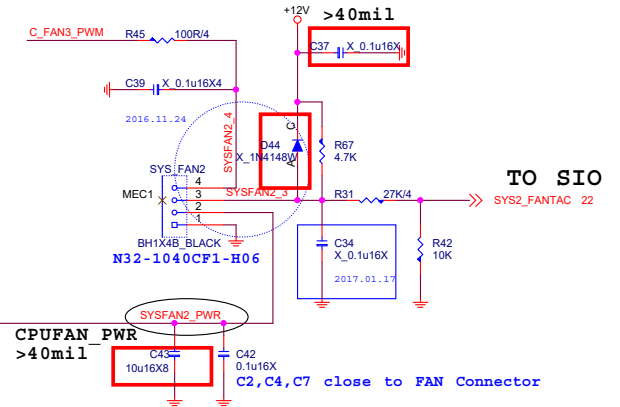


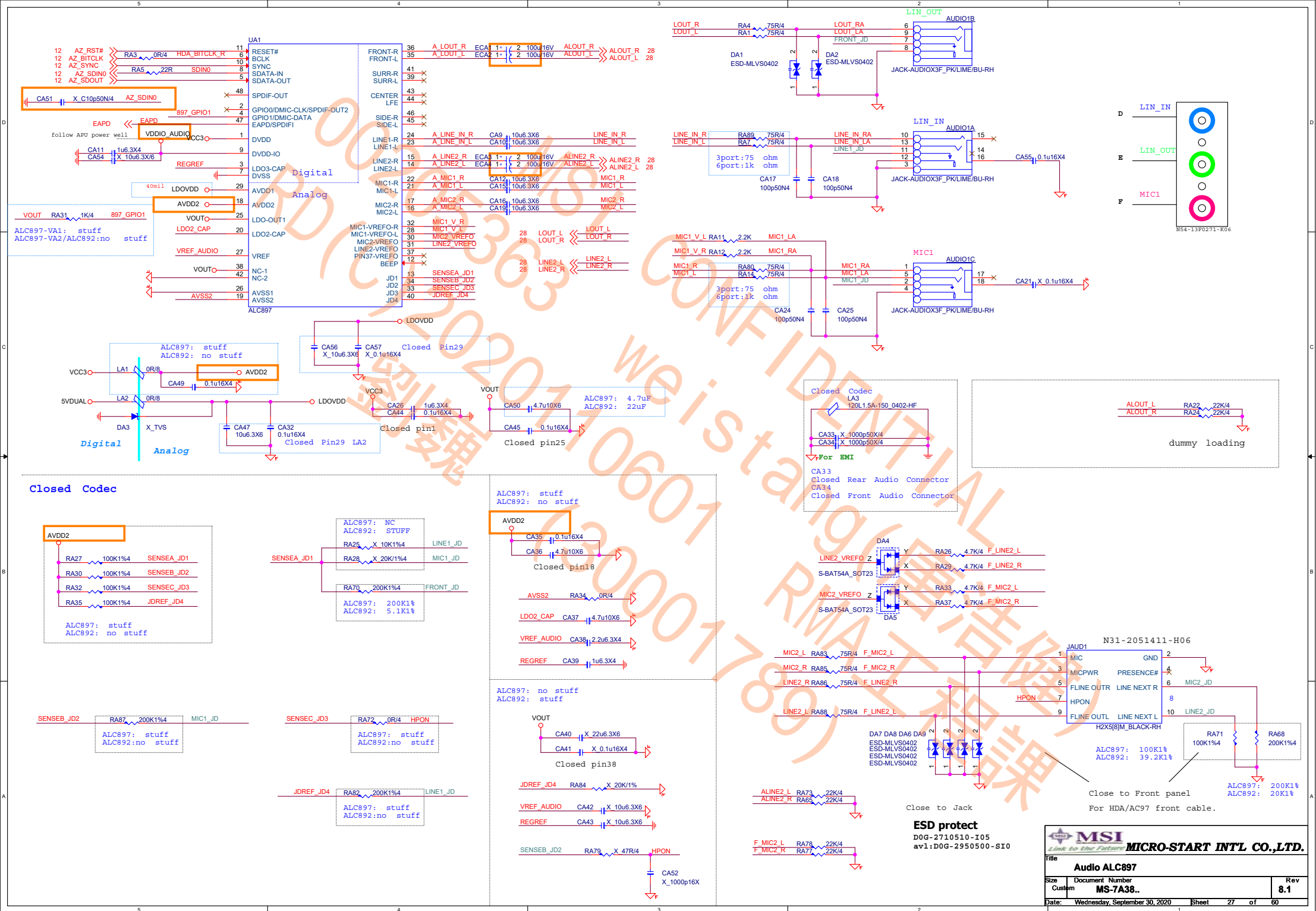
GPIO Control

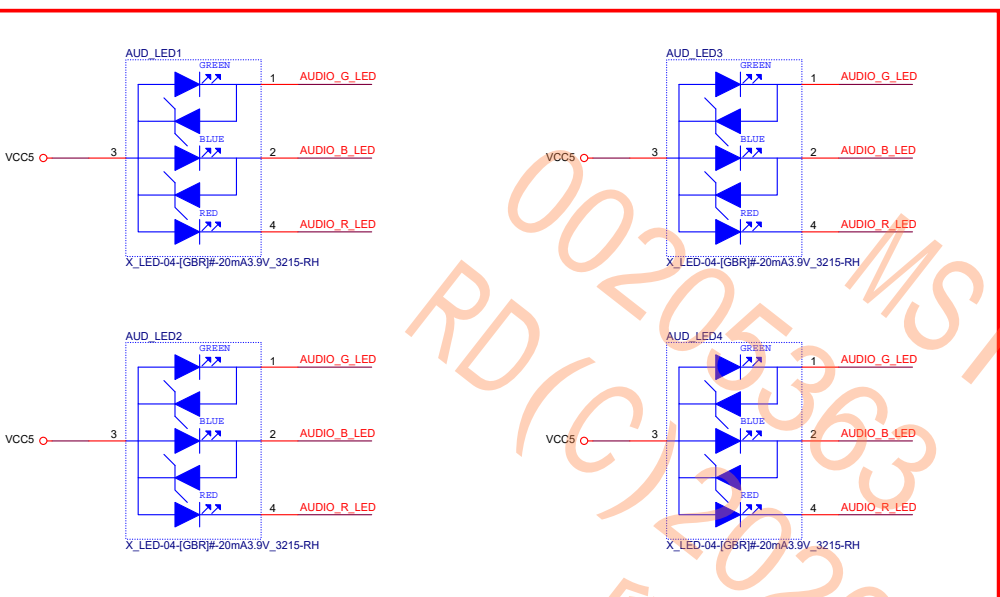
	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI (Floating)

Internall pull up 1.65V

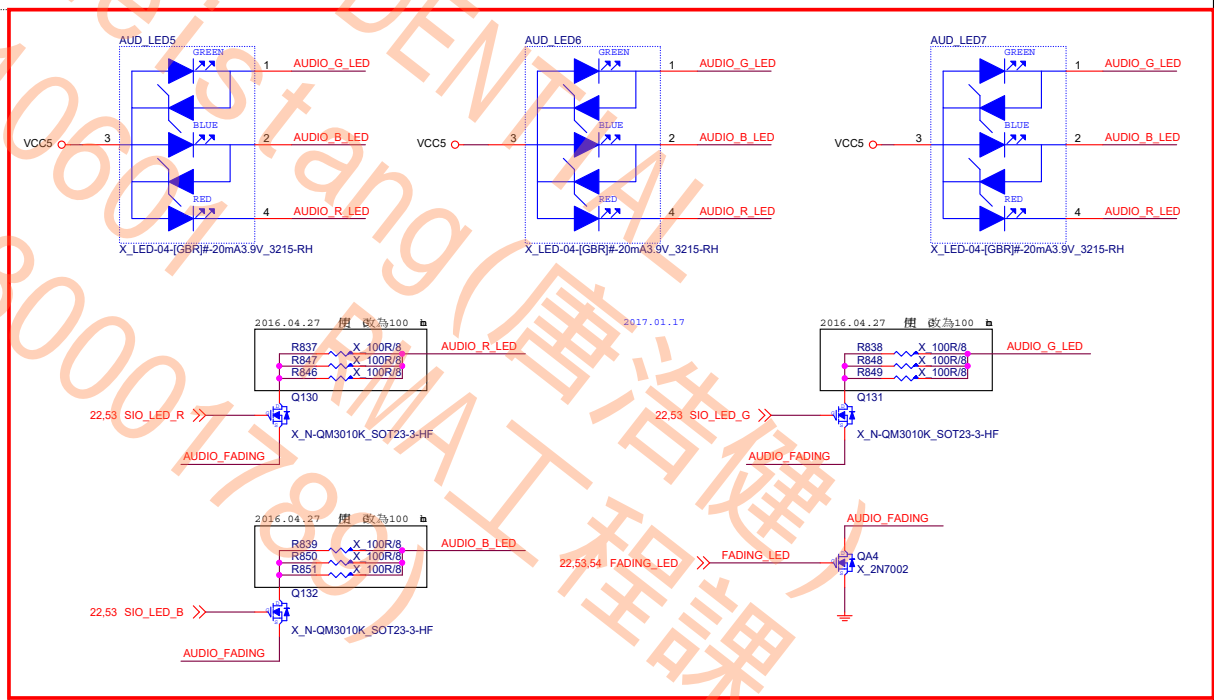
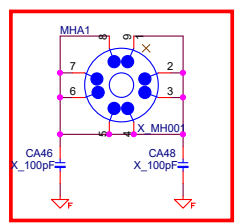
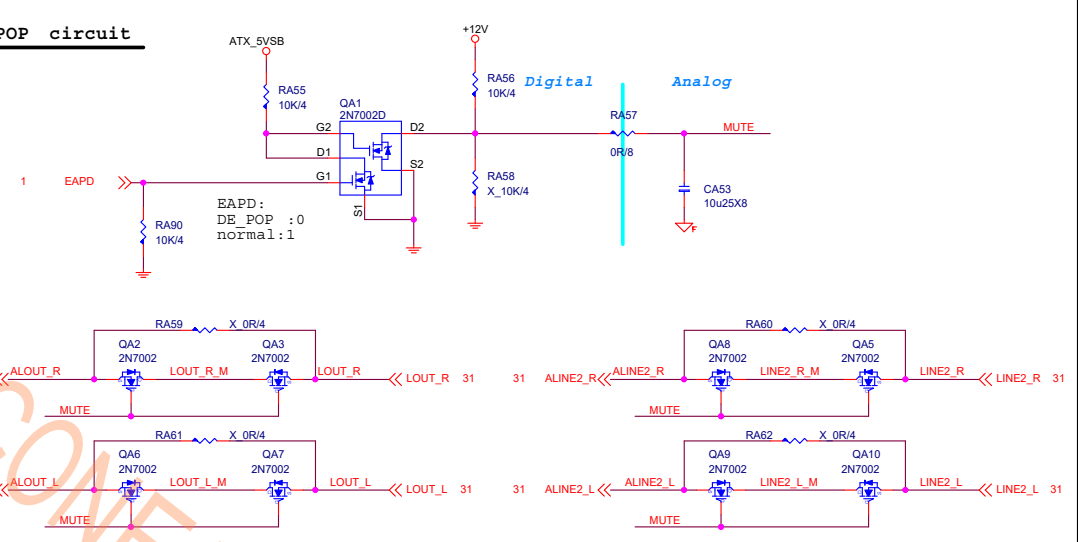
I22-3947S12-N62



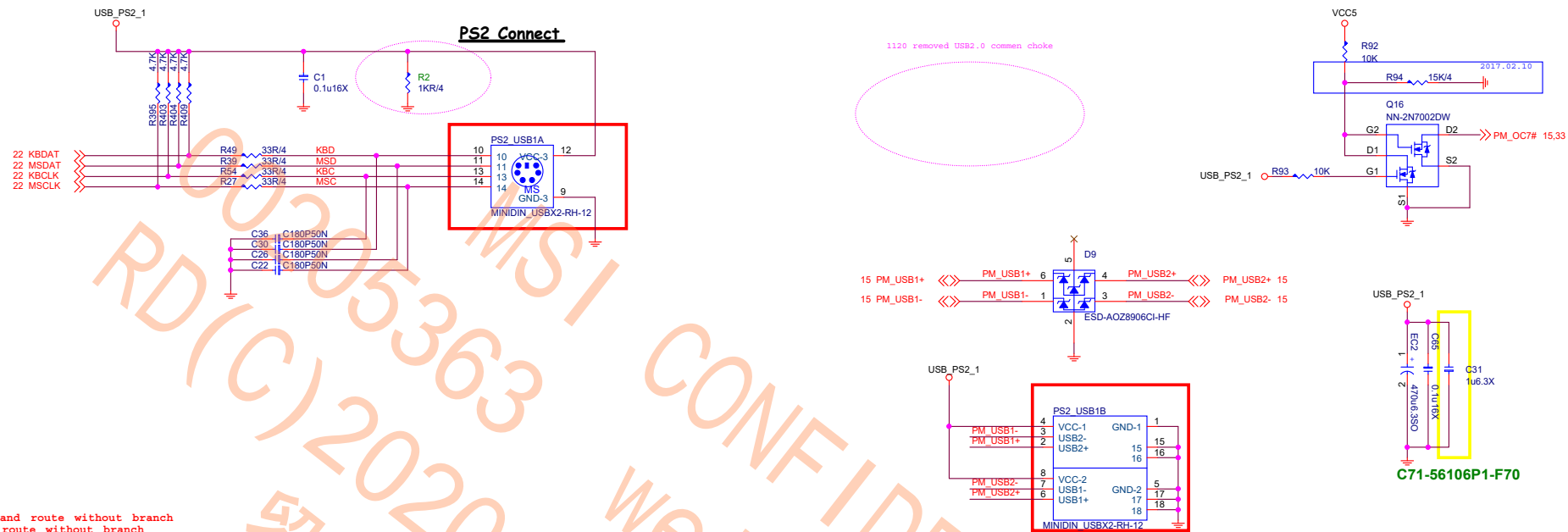




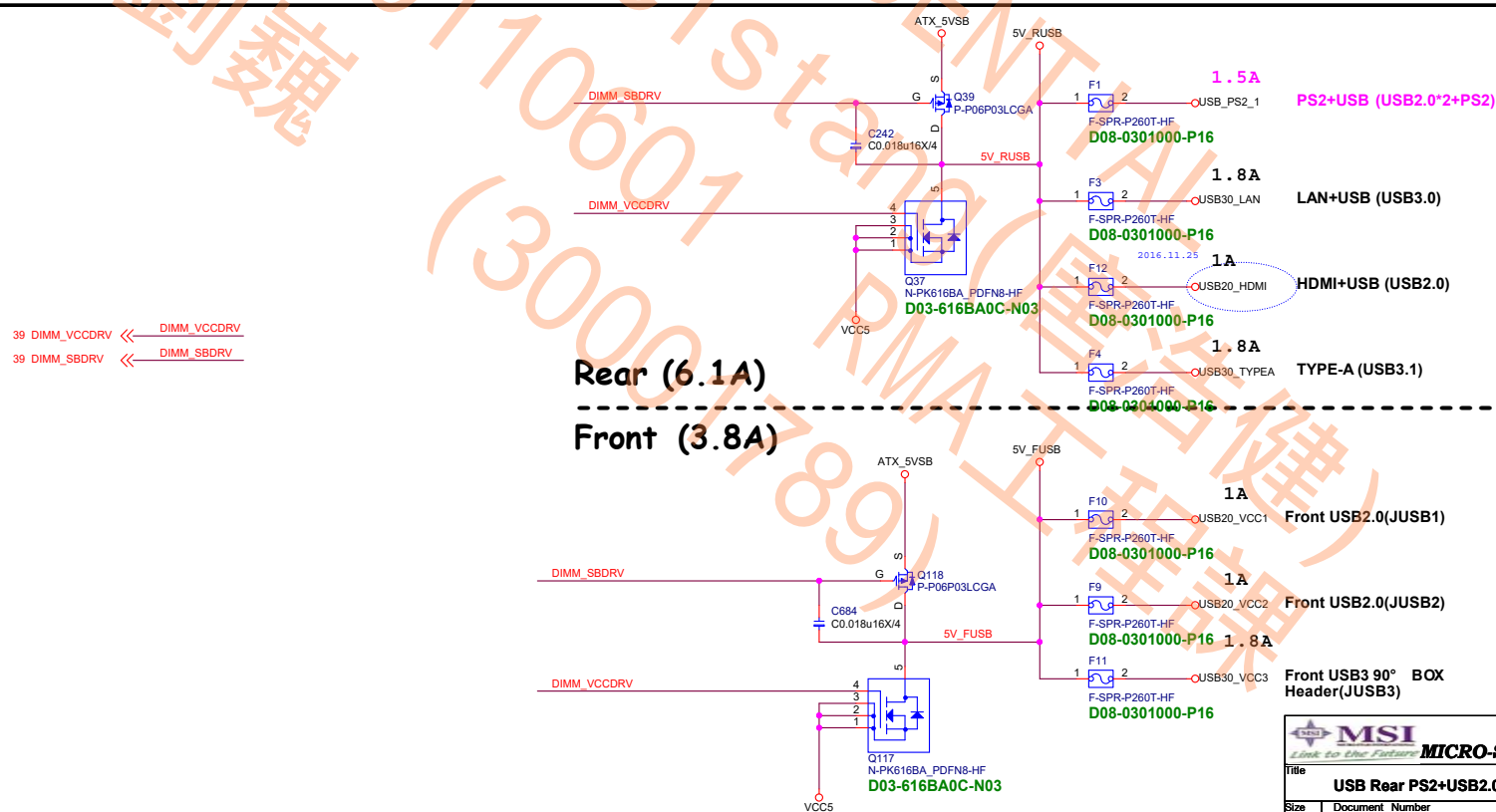
De-POP circuit



PS2+USB



USB Power



USB3.1 GEN1

VR Sloution U2 redriver

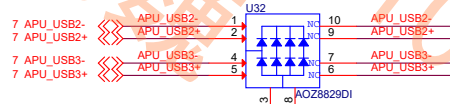
1120 removed USB2.0 common choke

7 APU_USB_SSTX2+ <<> C290 C0.22u6.3X APU_SSTX2+
7 APU_USB_SSTX2- <<> C293 C0.22u6.3X APU_SSTX2-

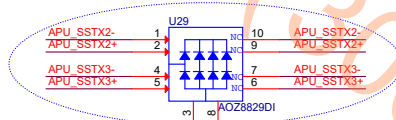
7 APU_USB_SSRX2+ <<> APU_USB_SSRX2+
7 APU_USB_SSRX2- <<> APU_USB_SSRX2-

7 APU_USB_SSTX3+ <<> C287 C0.22u6.3X APU_SSTX3+
7 APU_USB_SSTX3- <<> C288 C0.22u6.3X APU_SSTX3-

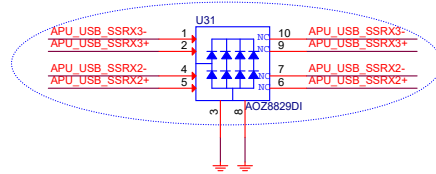
7 APU_USB_SSRX3+ <<> APU_USB_SSRX3+
7 APU_USB_SSRX3- <<> APU_USB_SSRX3-



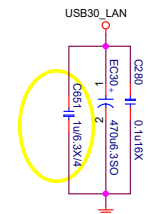
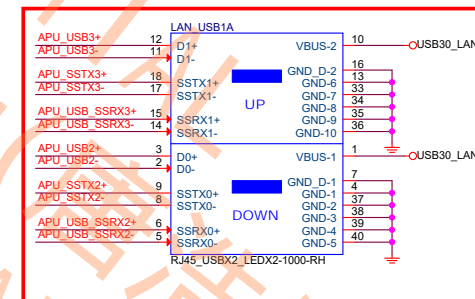
2016.12.01

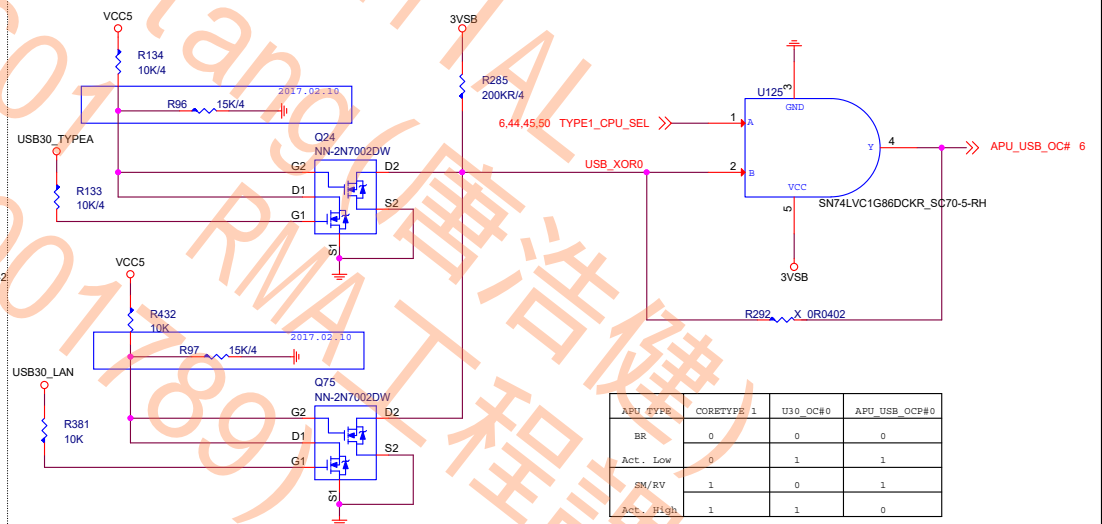
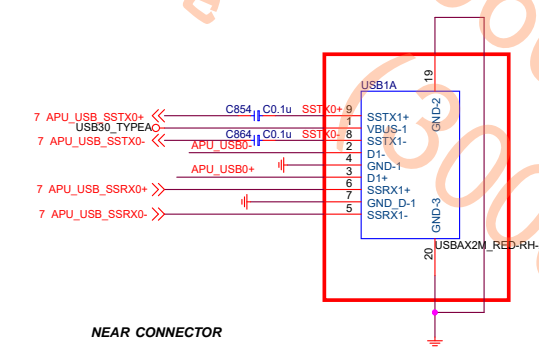
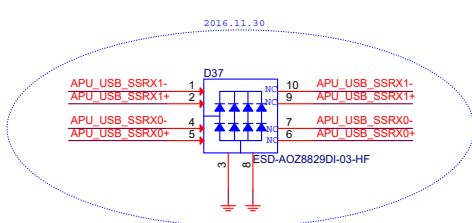
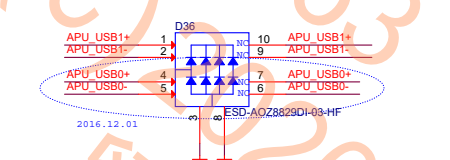
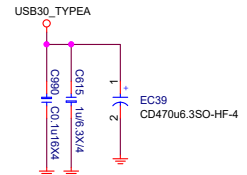


2016.12.01



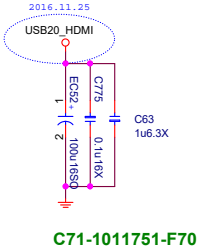
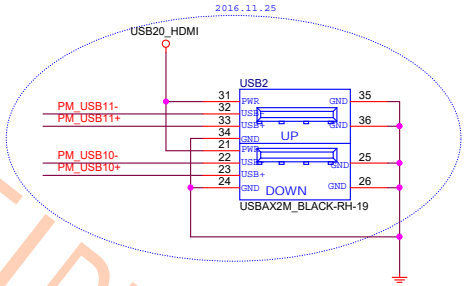
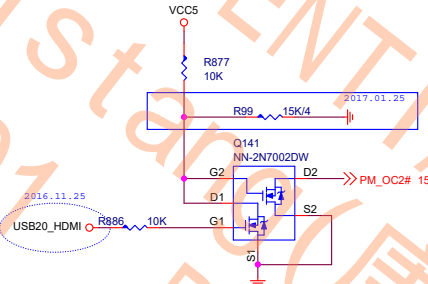
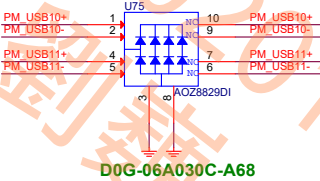
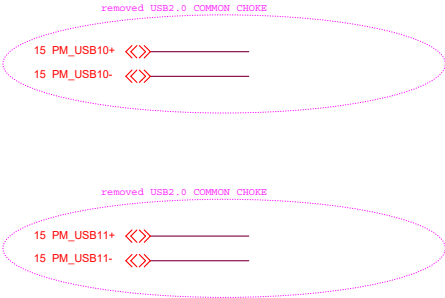
LAN+USB



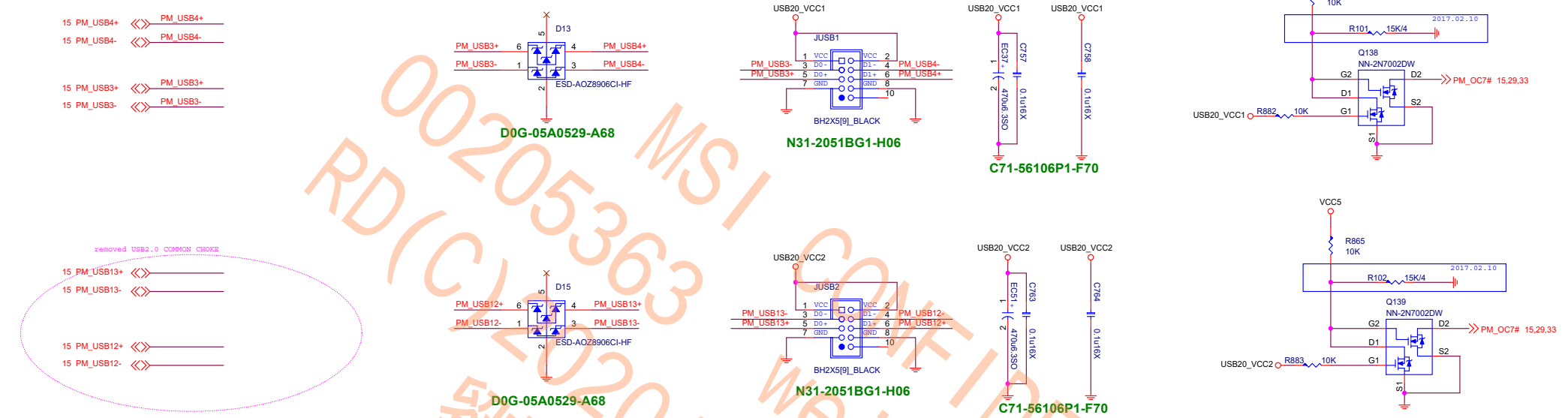


AFU TYPE	CORETYPE 1	U30_OC#0	AFU_USB_OCP#0
BR	0	0	0
Act. Low	0	1	1
SM/EV	1	0	1
Act. High	1	1	0

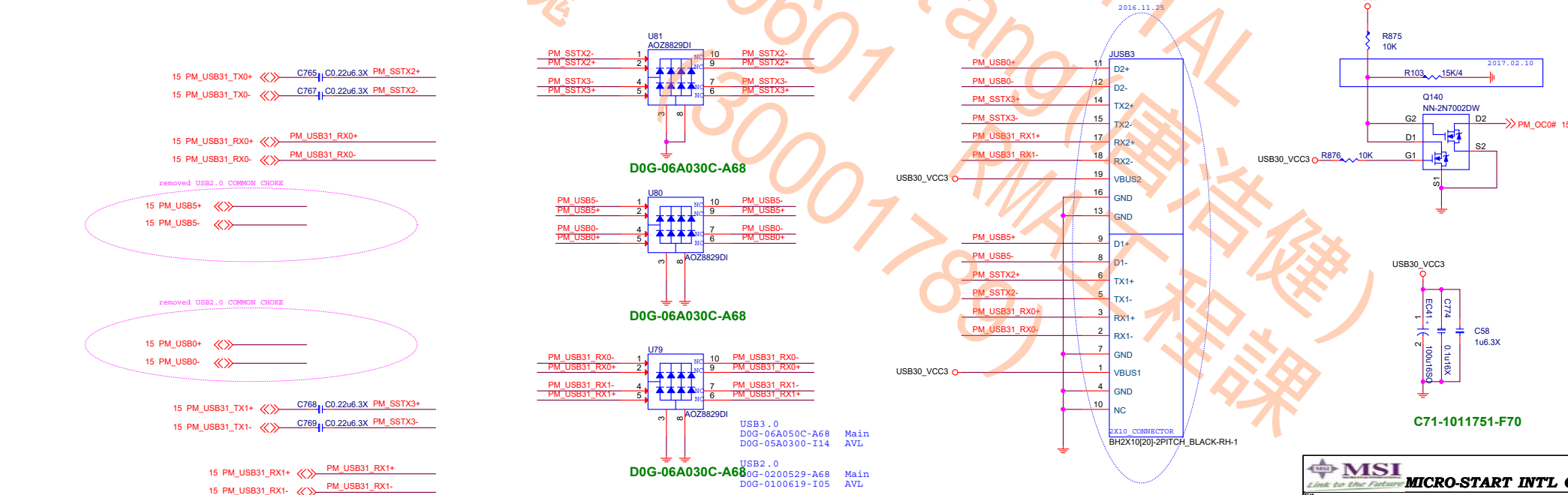
Front USB2.0



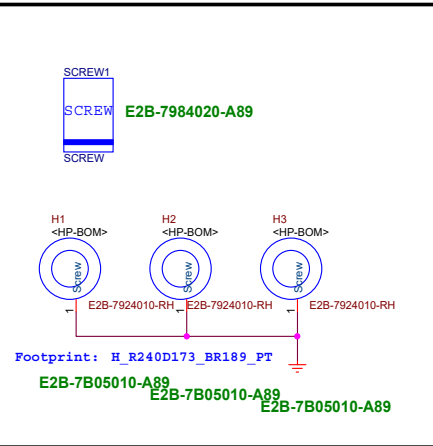
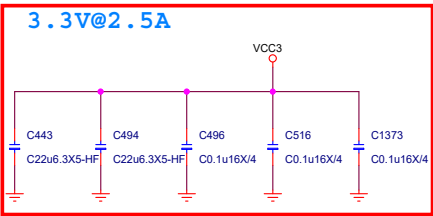
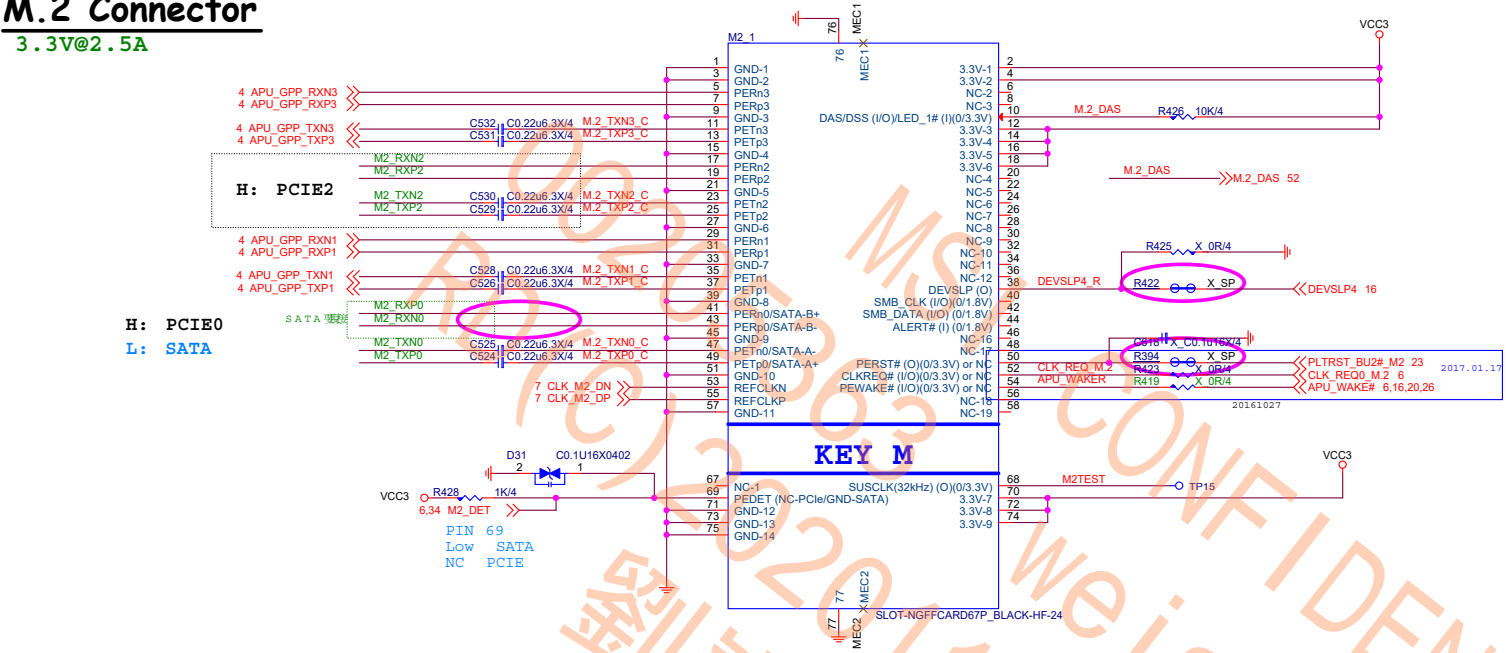
Front USB2.0



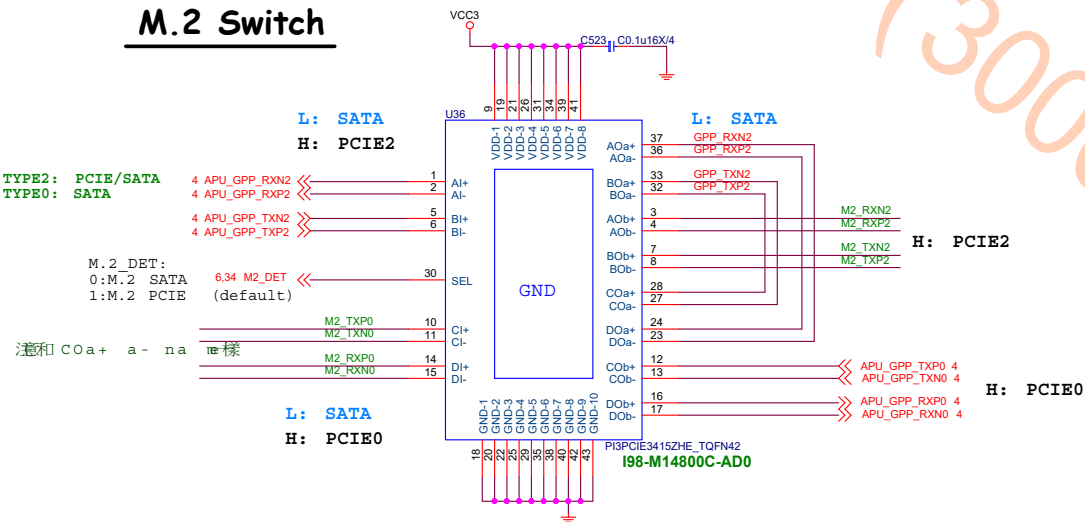
Front USB3.1 GEN1



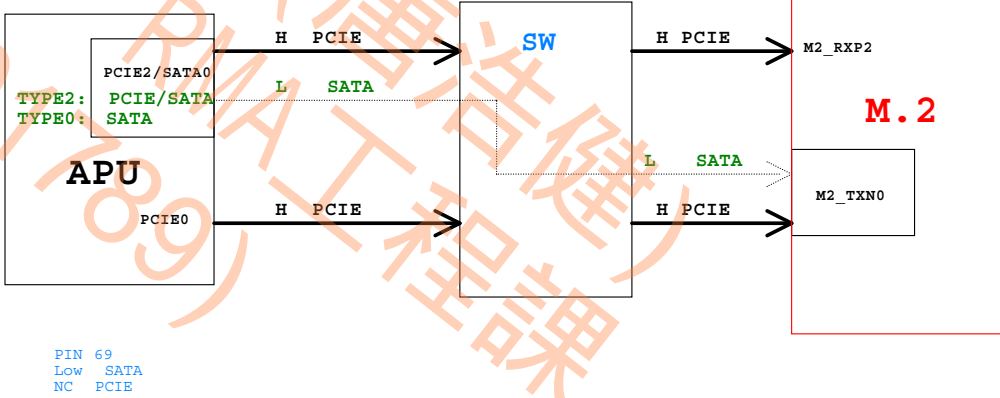
M.2 Connector
3.3V@2.5A



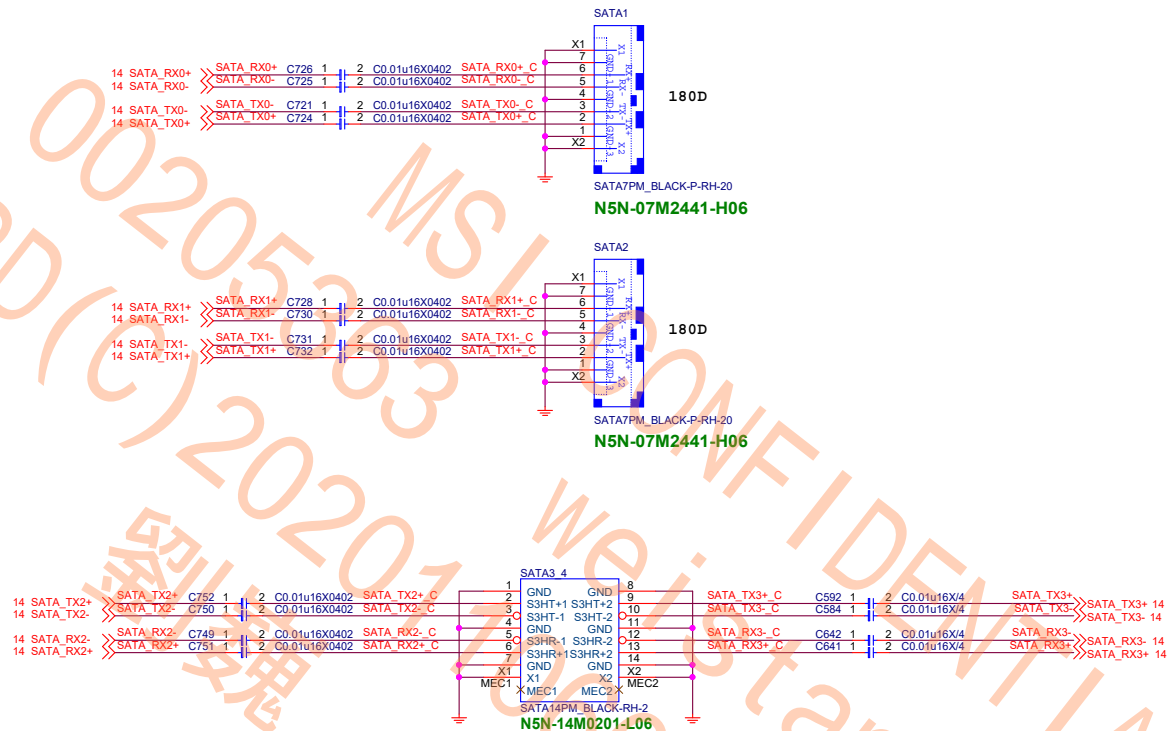
M.2 Switch



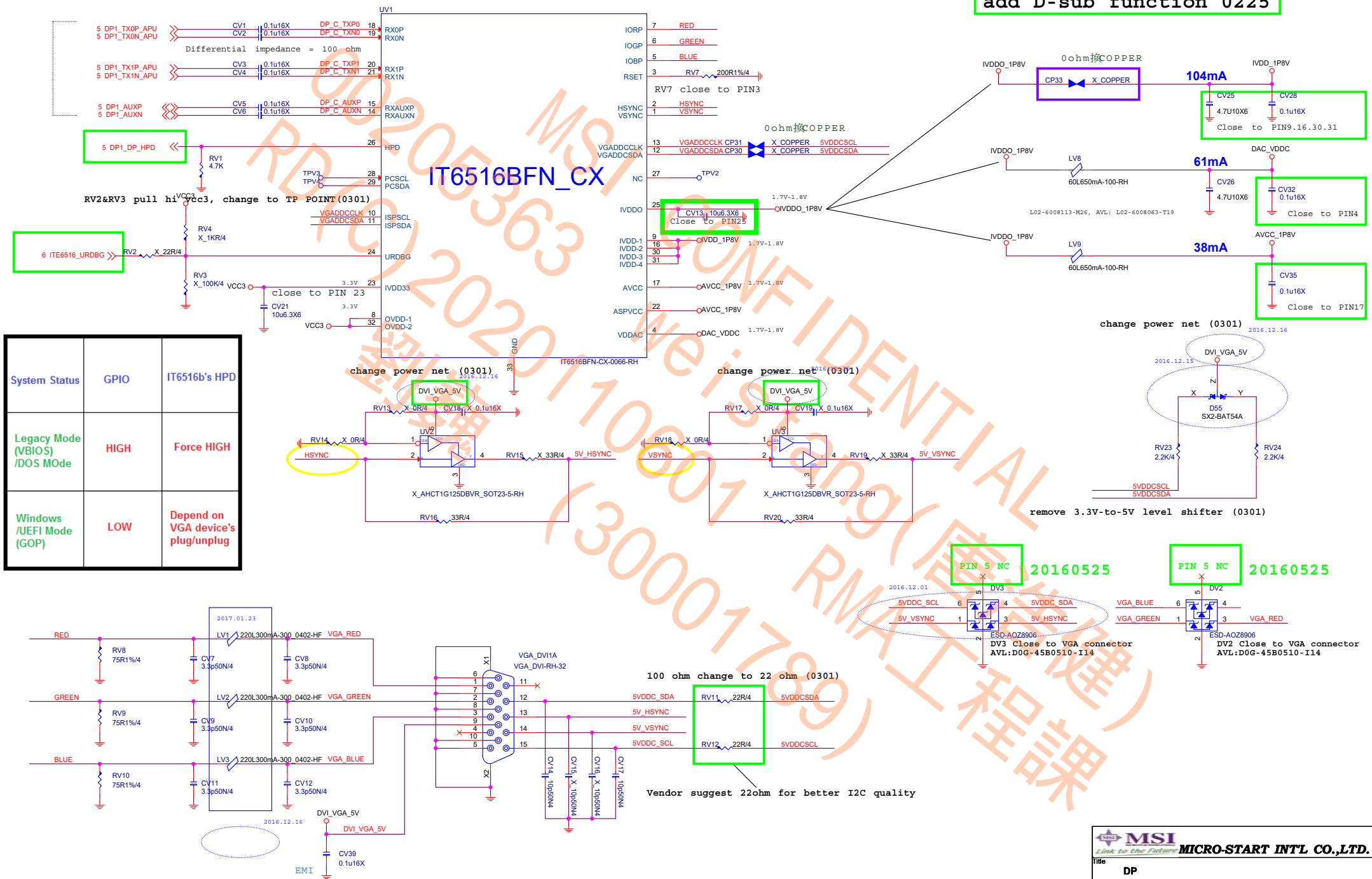
HW Default
M.2 Insert



SATA Connector

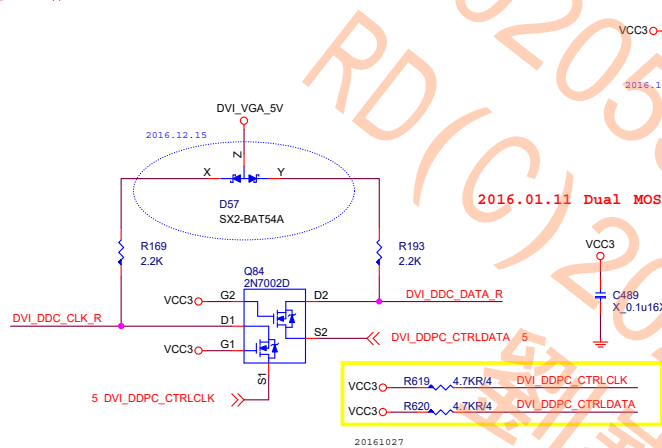
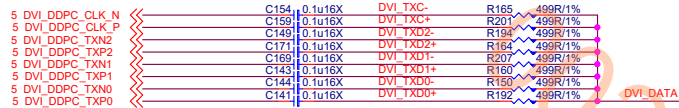


Note:
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

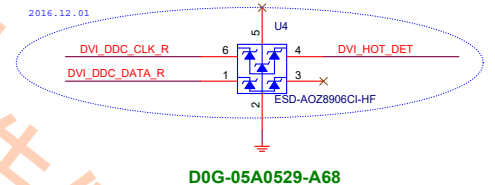
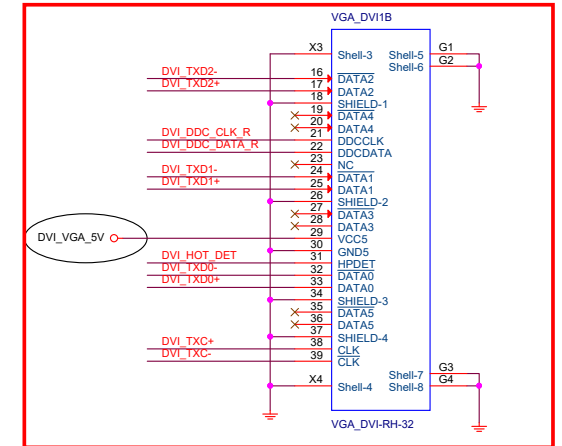
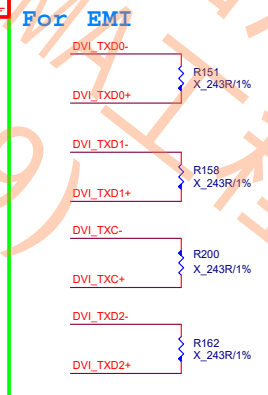
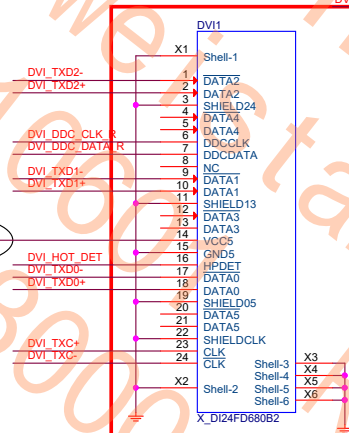
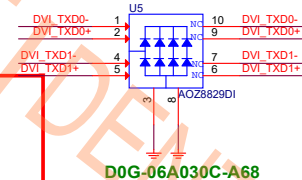
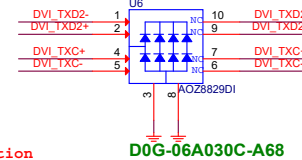
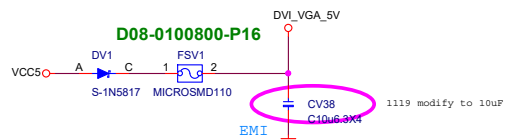
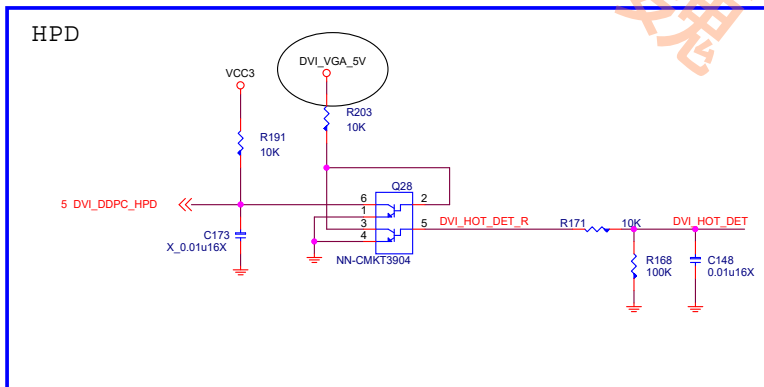


DVI level shifter

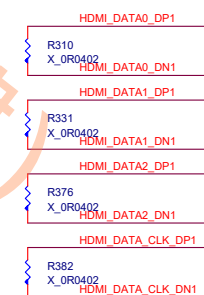
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



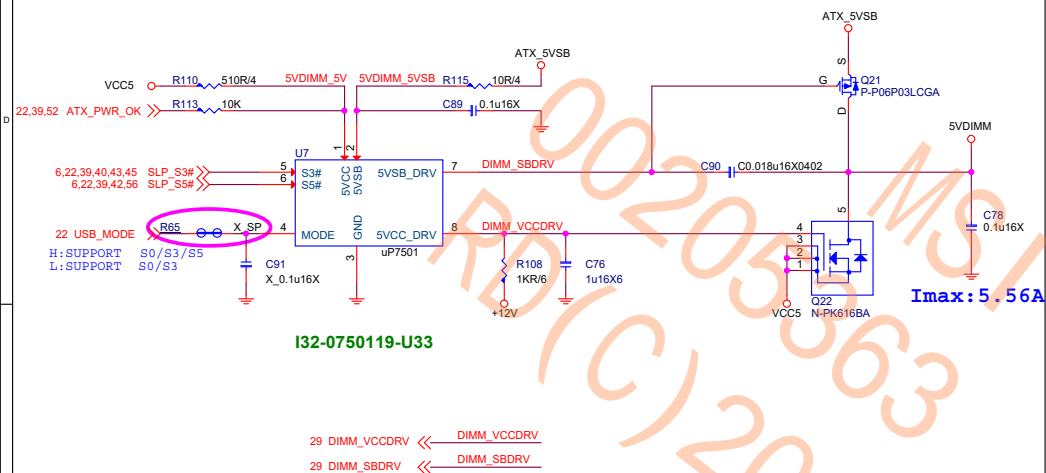
2016.01.11 Dual MOS change to single MOS, reduce CM noise by EMI Suggestion



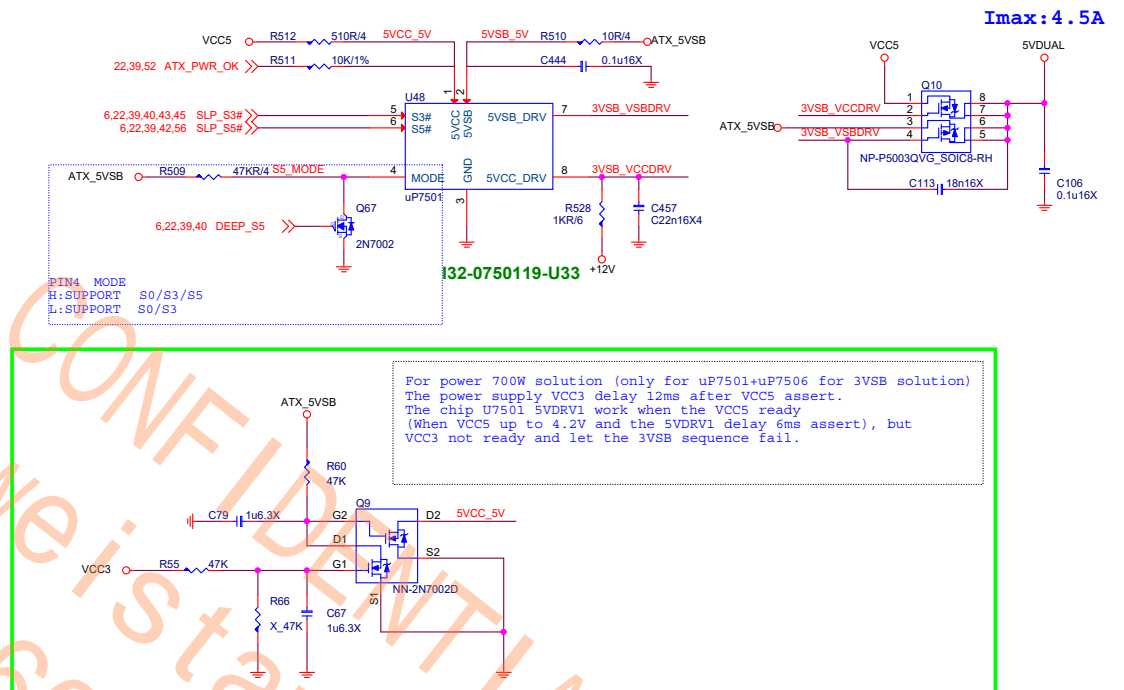
For HDMI 1.4



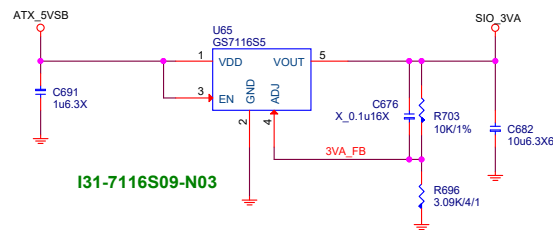
5VDIMM FOR DDR



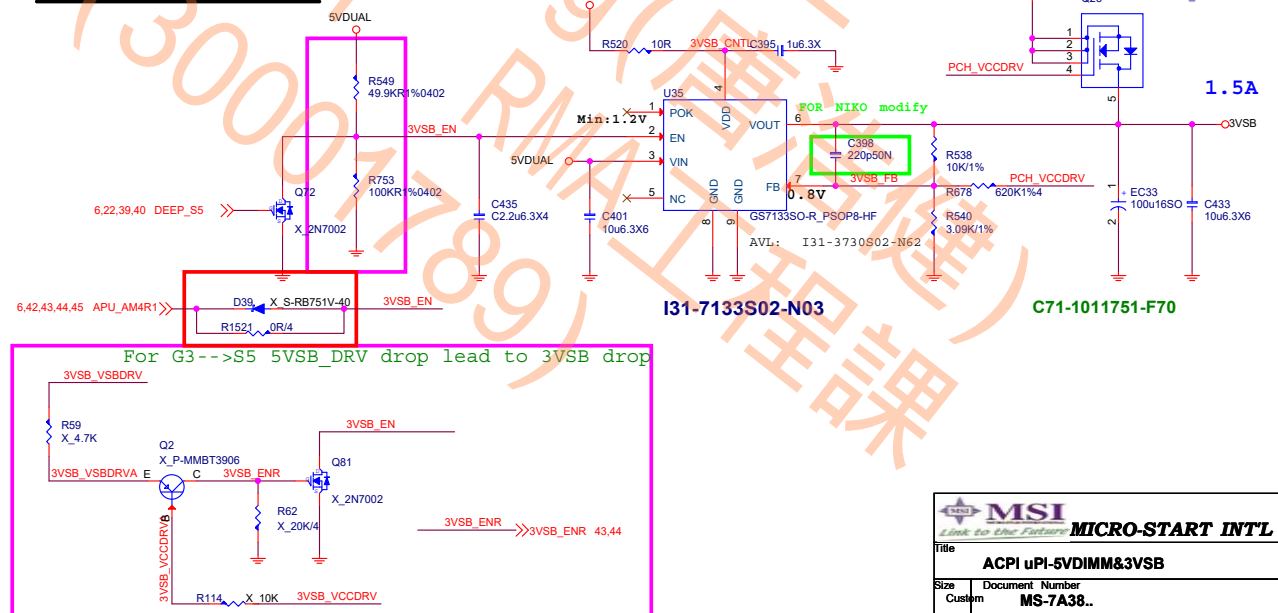
5VDUAL For 3VSB、CPU 1.8V、VDDP



SIO_3VA



3VSB cost down



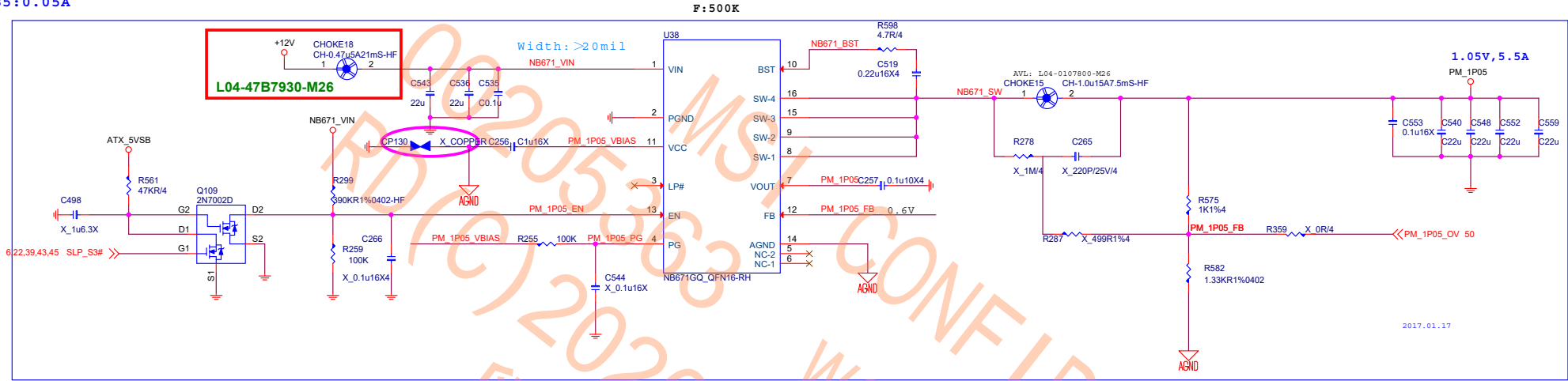
FOR Promontory 1.05V_S0

1.05V
S0:5.5A
S5:0.05A

support OV=>NB685
not support OV=> NB681

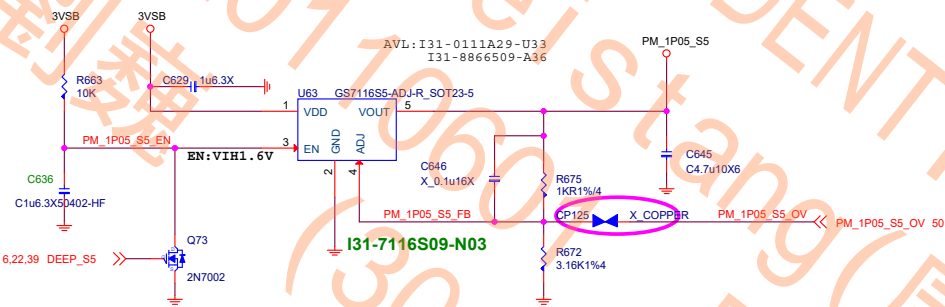
IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=13A~15A.
Output CHOKE Isat=15A

0.7776uH < 1.1664uH



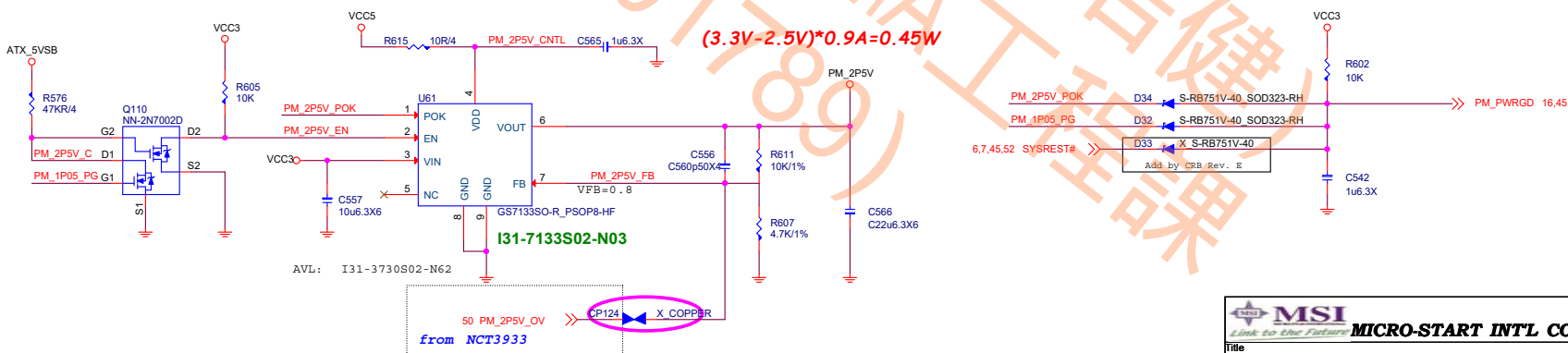
FOR Promontory 1.05V_S5

0.05A



Promontory-2.5V

2.5V; 900mA

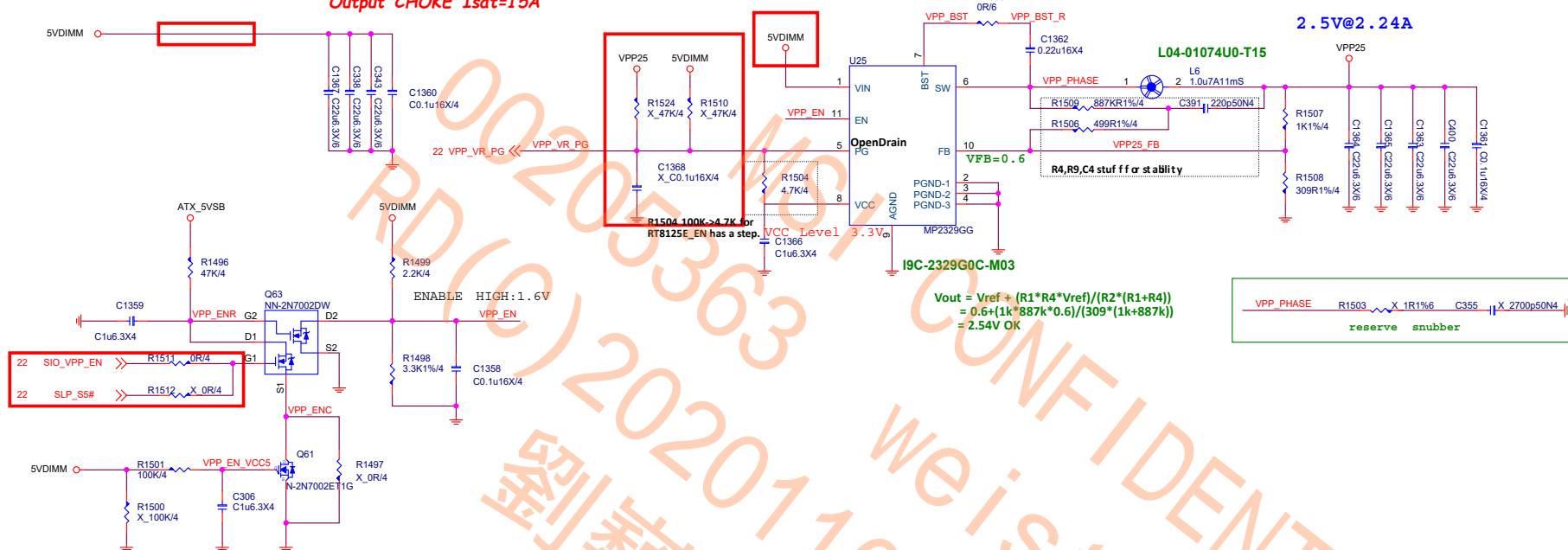


2.5V@2.24A

IMAX=2.24A
ILIMIT=7.5A
IOC=ILIMIT+40%*IMAX/2=7.948A.
Output CHOKE Isat=15A

VPP BST VPP BST R >50 mils.

2.5V@2.24A

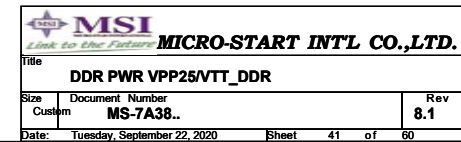
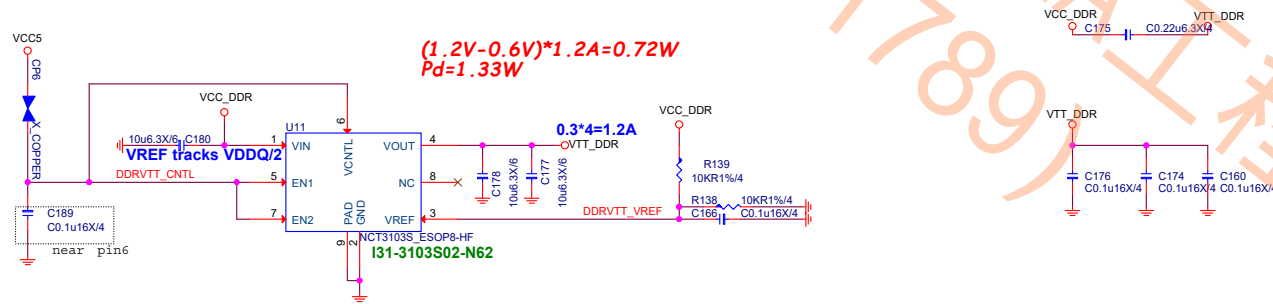


$$\begin{aligned} V_{out} &= V_{ref} + (R1 \cdot R4 \cdot V_{ref}) / (R2 \cdot (R1 + R4)) \\ &= 0.6 + (1k \cdot 887k \cdot 0.6) / (309 \cdot (1k + 887k)) \\ &= 2.54V \text{ OK} \end{aligned}$$

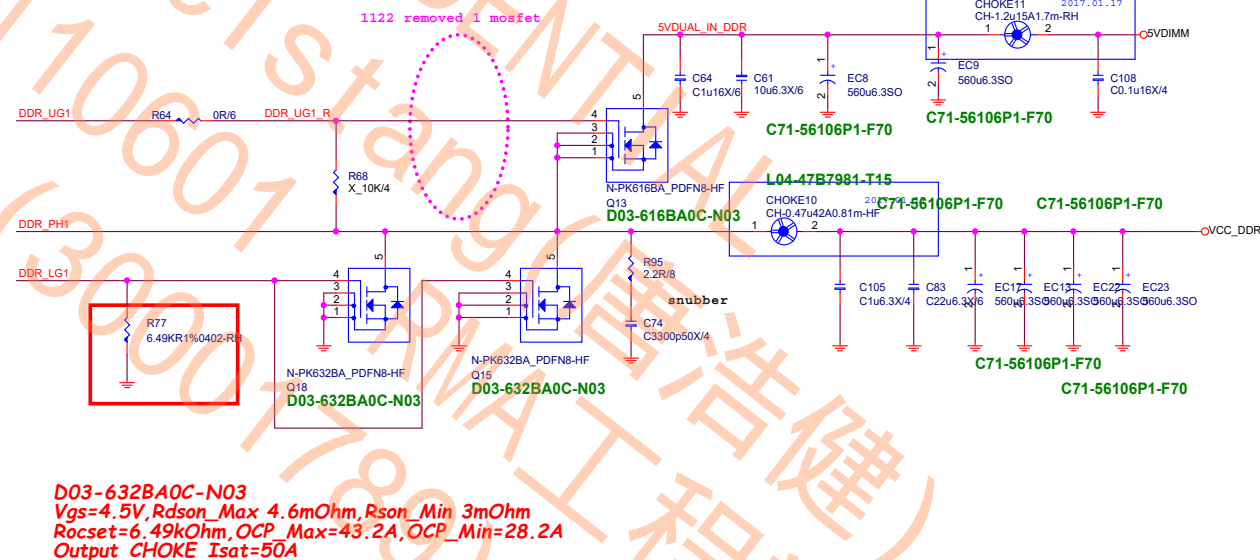
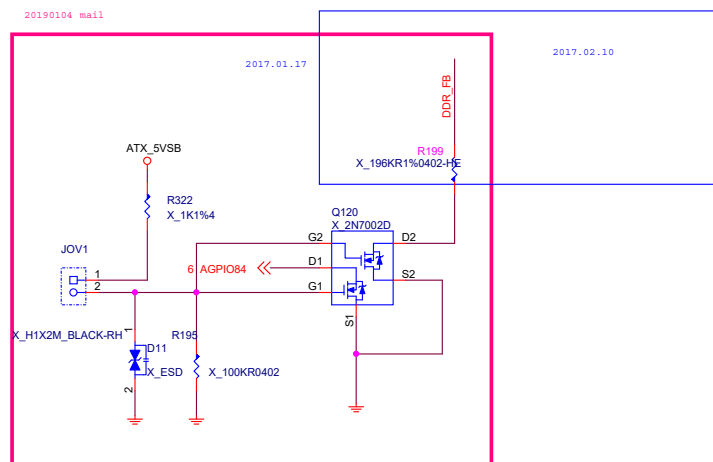
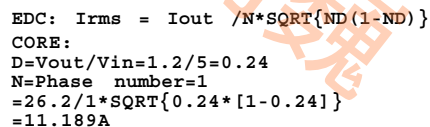
reserve snubber

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

$$(1.2V - 0.6V) * 1.2A = 0.72W$$
$$P_d = 1.33W$$



15.5A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT



D03-632BA0C-N03
Vgs=4.5V, RdsOn_Max 4.6mOhm, Rson_Min 3mOhm
Rocset=6.49kOhm, OCP_Max=43.2A, OCP_Min=28.2A
Output CHOKE Isat=50A

CPU 1P8 S5

CPU: VDD 18_S5@0.5A
CPU: VDDIO_Audio@0.25A
CHIP: VDD_18_S5@0.1A

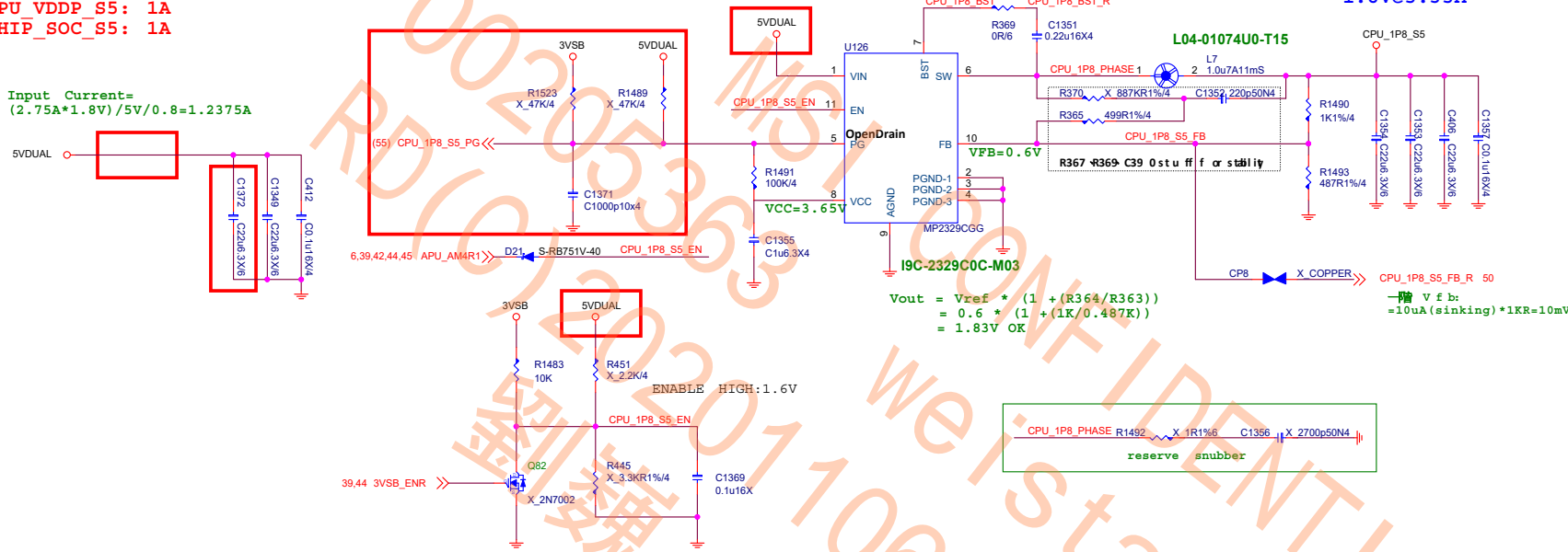
CPU_1P8: 2.5A
CPU_VDDP_S5: 1A
CHIP_SOC_S5: 1A

IMAX 5.35A
ILIMIT=6~9A
IOC=ILIMIT+40%*IMAX=7.07~10.07A.
Output CHOKE Isat=12A

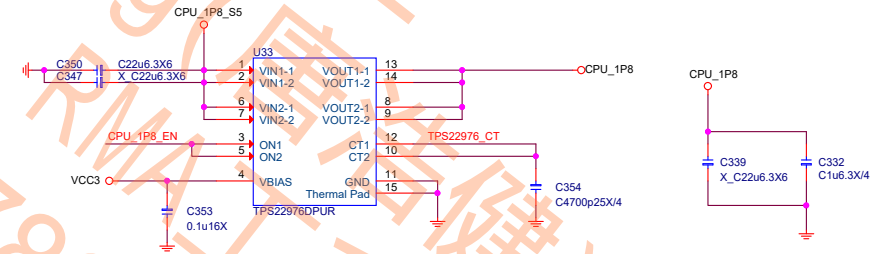
CPU_1P8_BST CPU_1P8_BST_R >50 mils.

1.8V@5.35A

Input Current=
(2.75A*1.8V)/5V/0.8=1.2375A

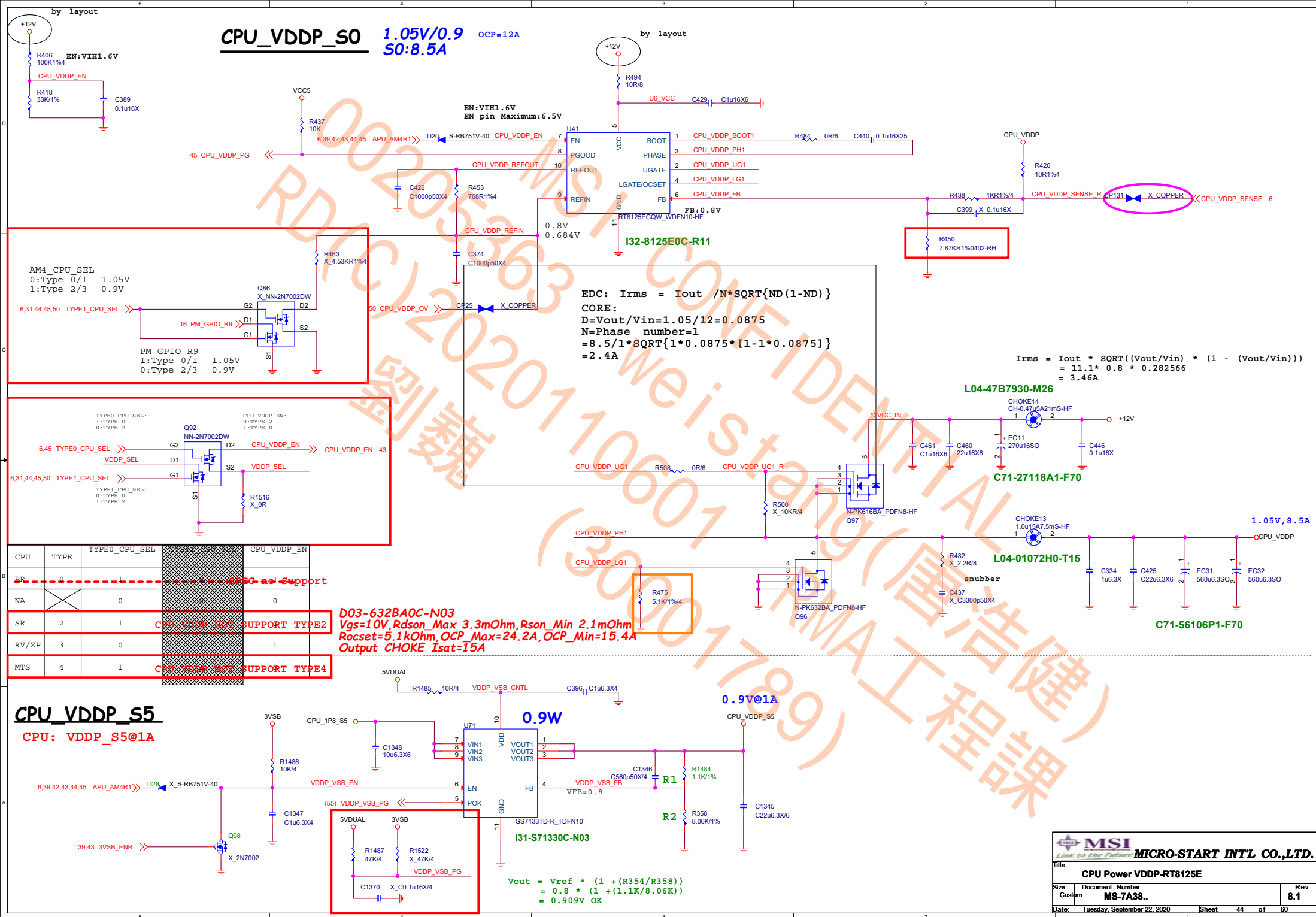


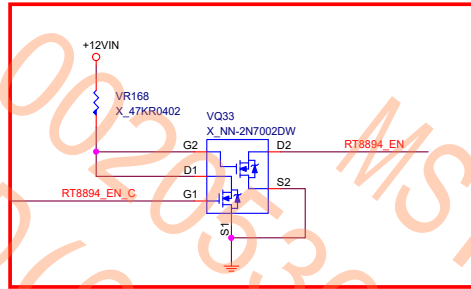
2.5A*2.5A*22mOhm=0.1375W



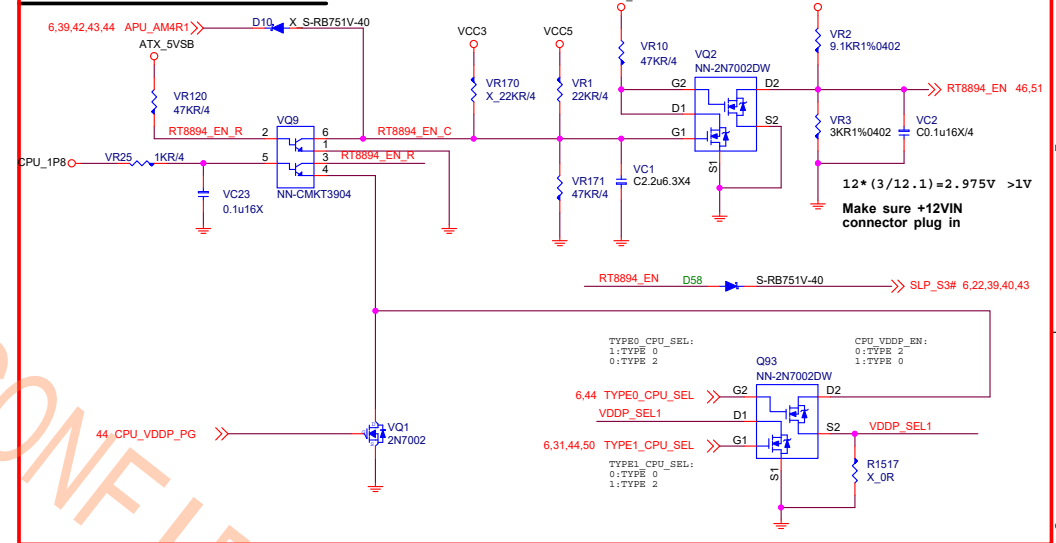
Adjustable Rise Time
SR = 0.42*CT+66
SR is the slew rate in (μs/V)
CT is constant value on CT pin (in pF)
The units for the constant 66 is in (μs/V)

DDR_PWRGD --> CPU_VDDP_EN
DDR_PWRGD --> CPU_1P8

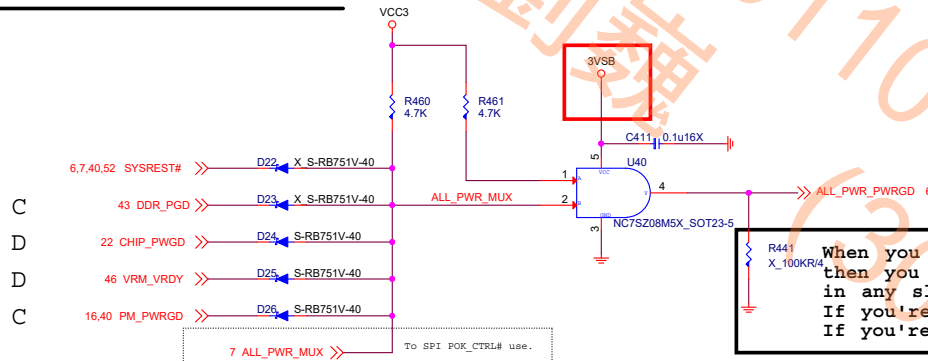




VRM_Enable circuit



ALL POWER GOOD MUX

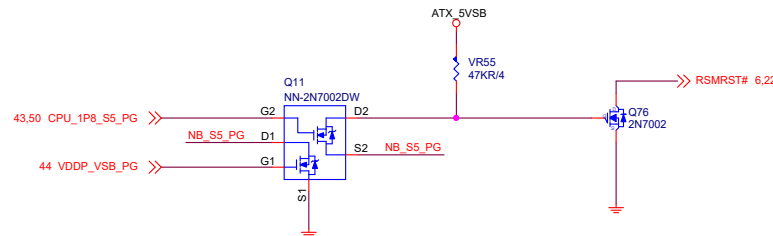


When you use external buffer then you cannot let APU PWR_GOOD pin float in any sleep state. If you're buffer use 3.3V_S0 and you need Pull-down 100K. If you're buffer use 3.3V_S5 and you don't need PD.

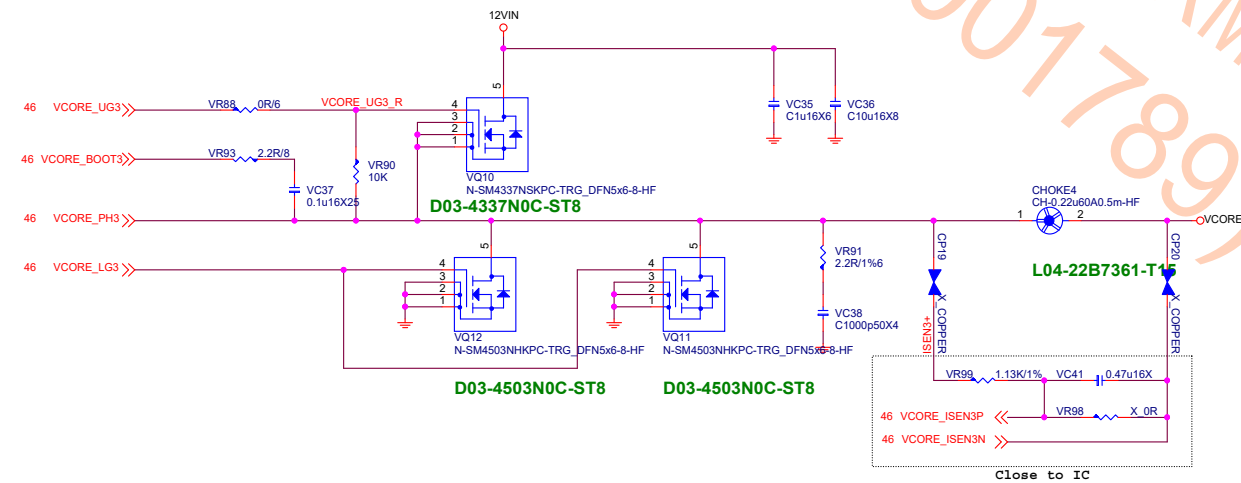
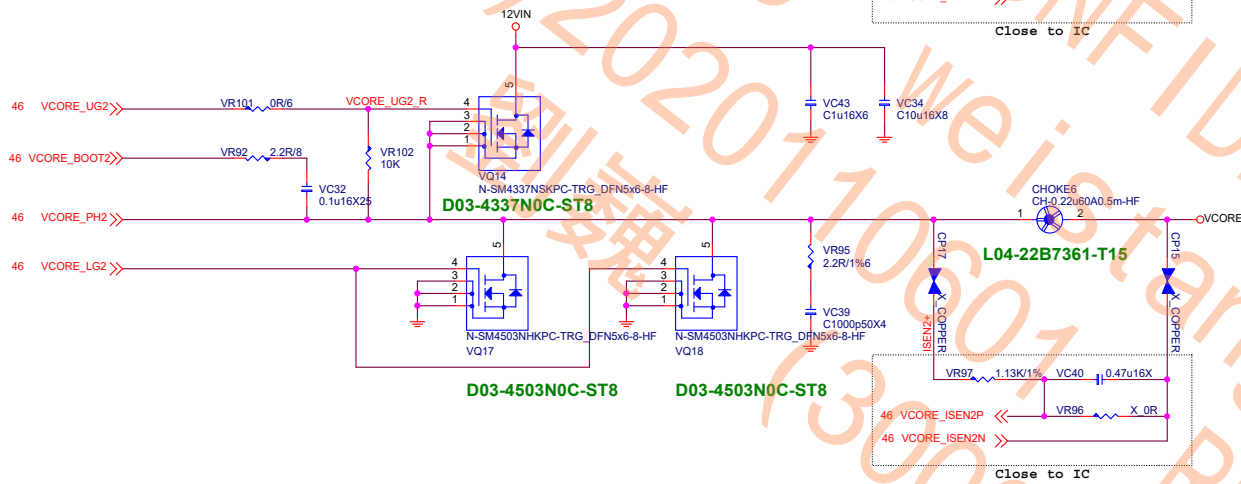
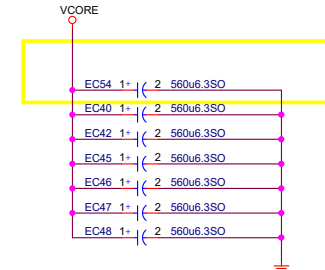
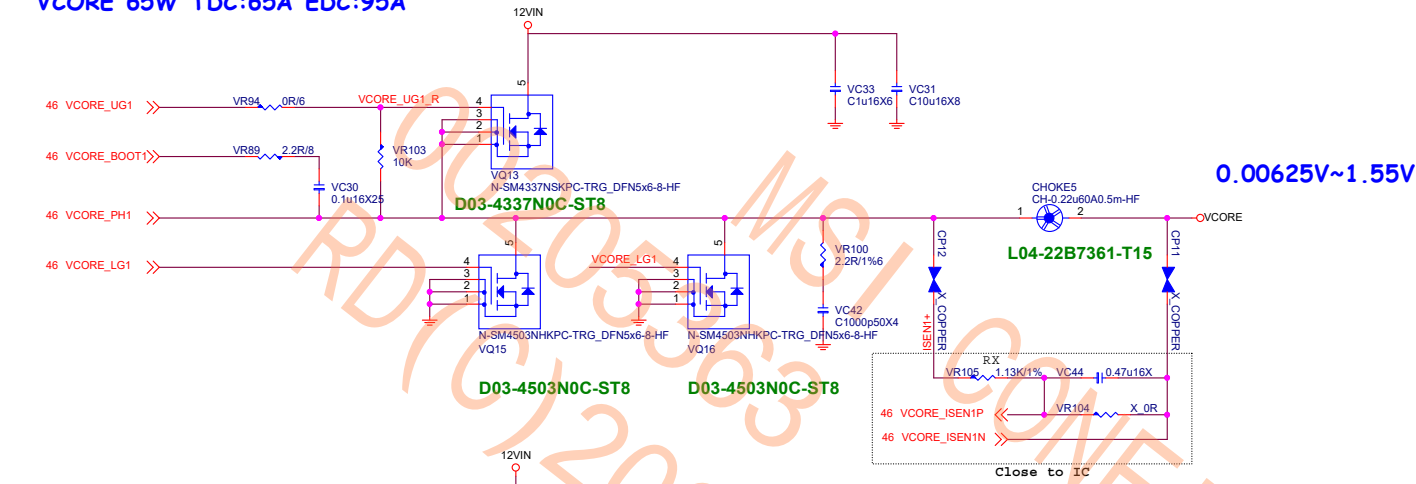
CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
NA		0	0
SR	2	CPU VDDP ¹ NOT SUPPORT TYPE2	
RV/ZP	3	1	0
MTS	4	CPU VDDP ¹ NOT SUPPORT TYPE4	

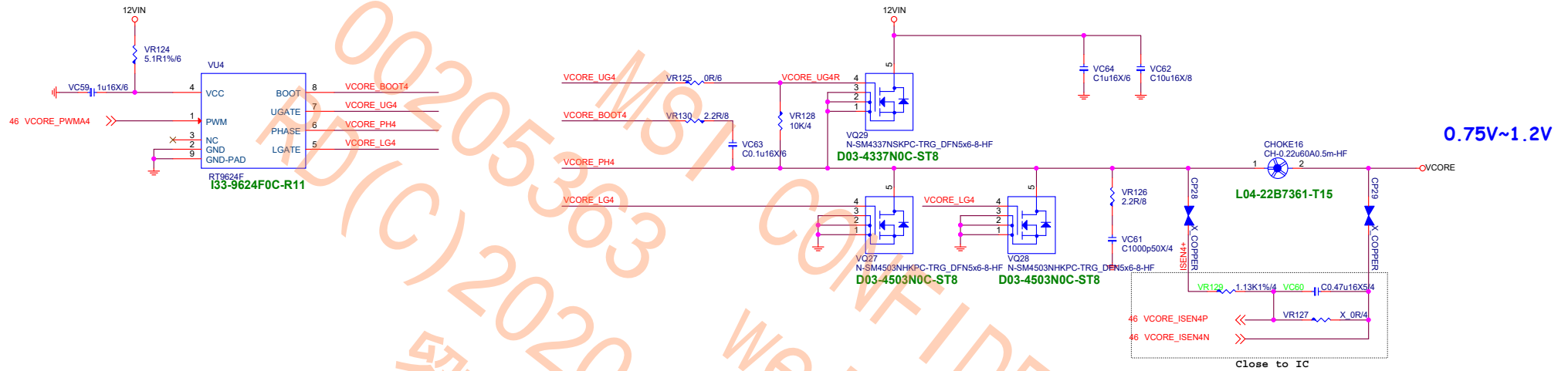
S0 PG

S5 PG

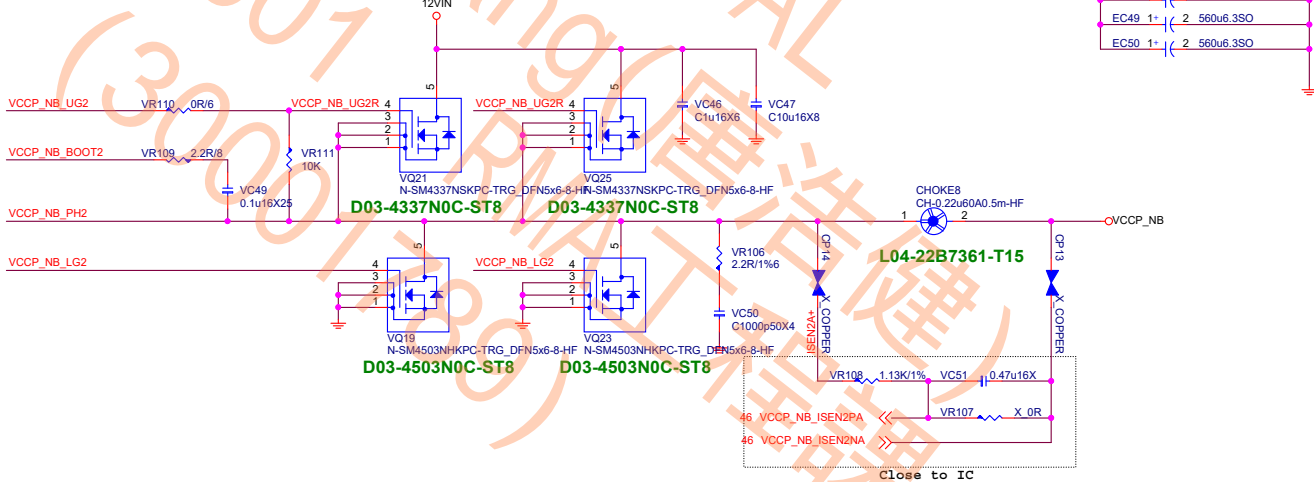
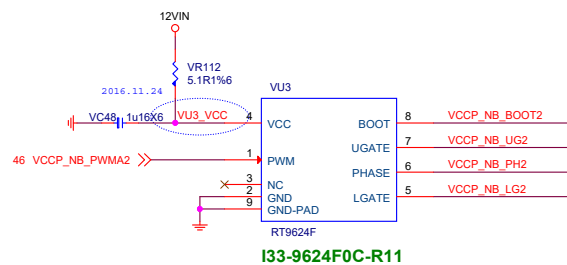
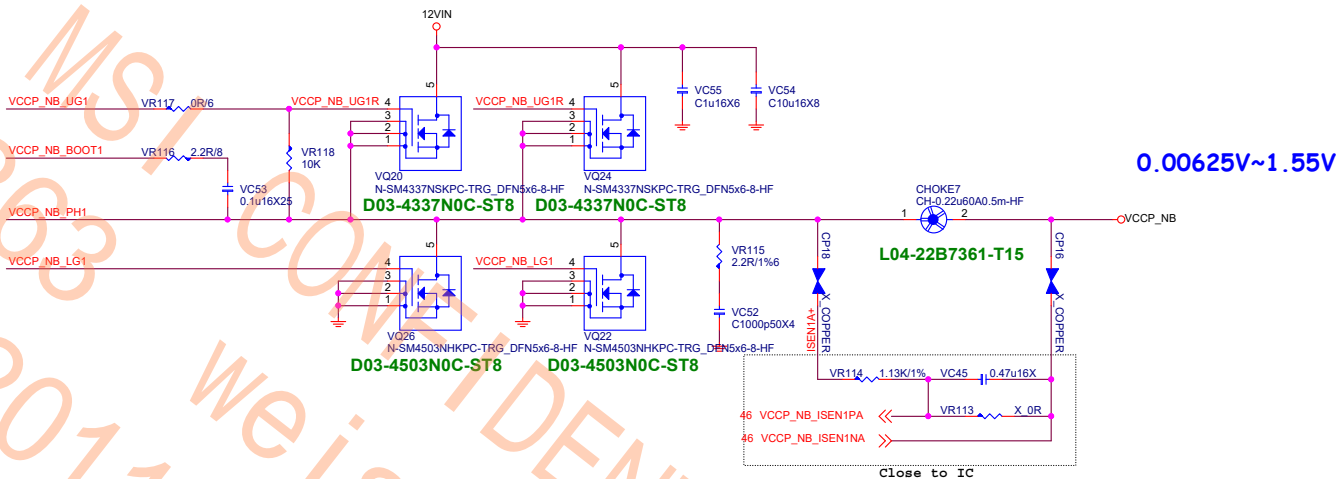
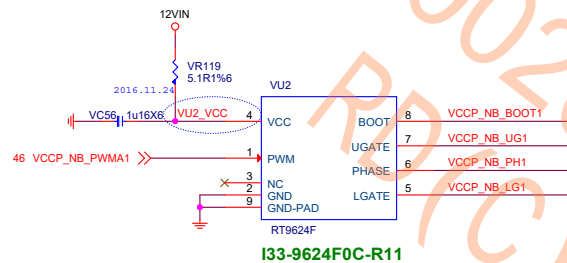


VCORE 95W TDC:80A EDC:125A
VCORE 65W TDC:65A EDC:95A





VCCP_NB 95W TDC:50A EDC:75A
VCCP_NB 65W TDC:50A EDC:75A



FOR VCCP_SOC_S5
0.9A

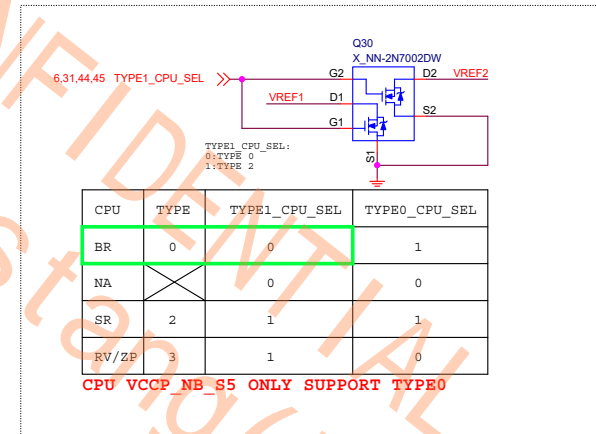
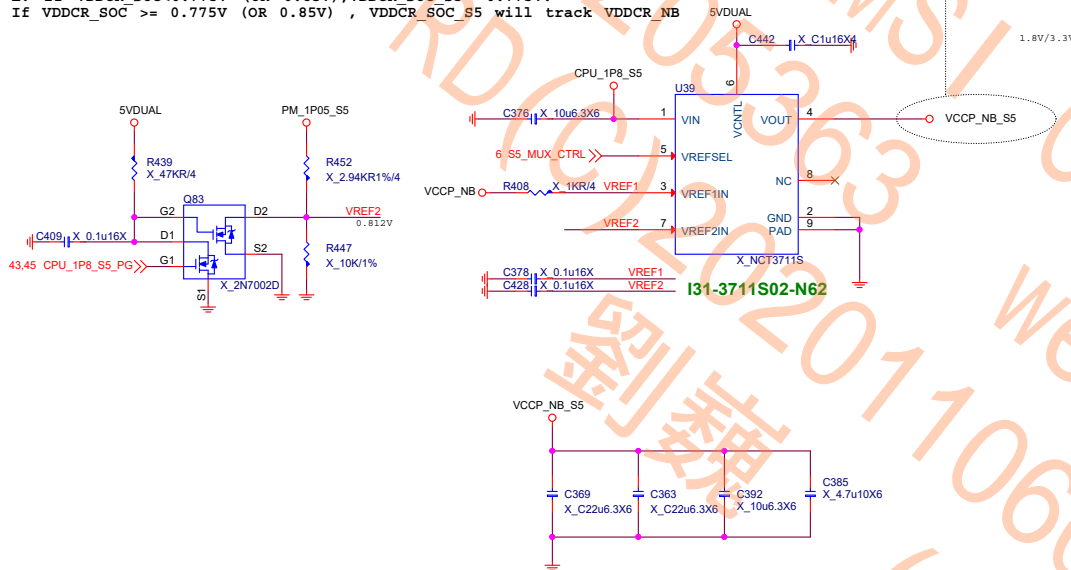
Do not Support Bristol,
Remove VCCP_NB_S5.

TYPE0 Only

S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V), VDDCR_SOC S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC S5 will track VDDCR_NB

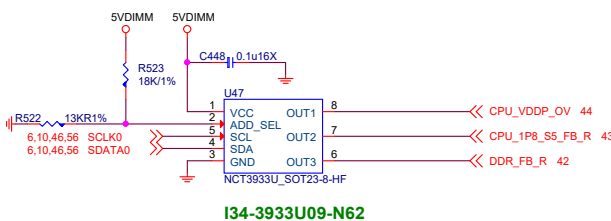
(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors)Bristol Ridge TYPE0



Over Voltage Control IC

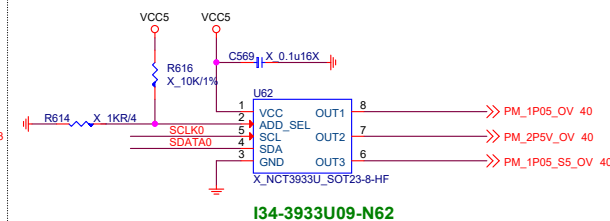
UPI VOLTAGE CONSOLE

0x26: RH=18K, RL=13K

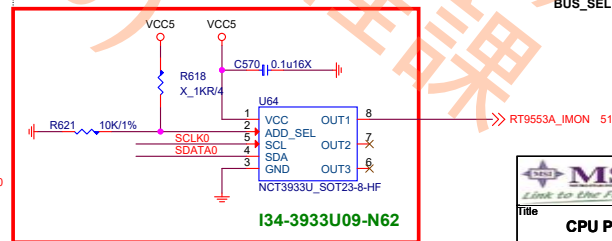


除非設置功能有任何幫助,否則不上NCT3933與開起點選項

0x20: RH=10K, RL=OPEN



0x2A: RH=OPEN, RL=10K



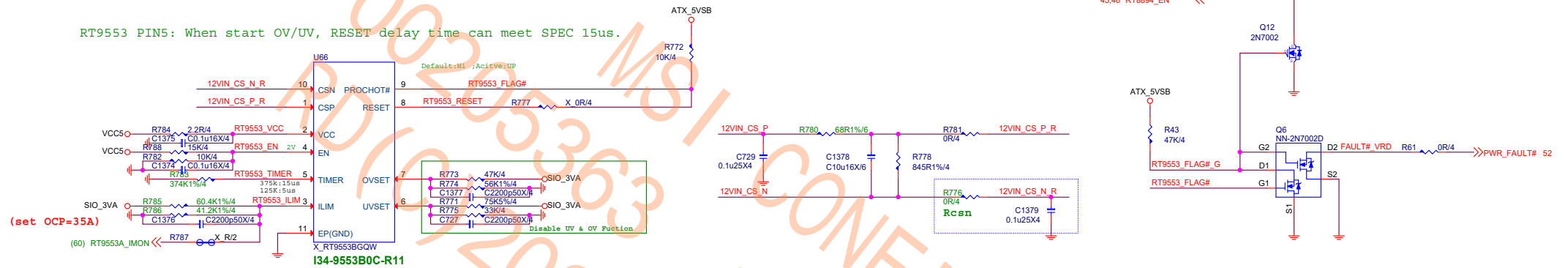
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

RT9553 CURRENT SENSE

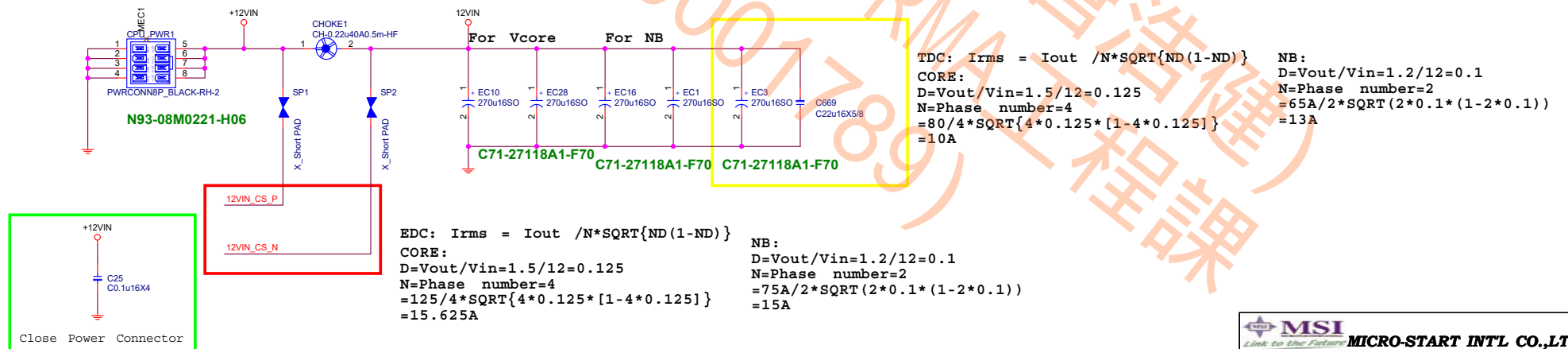
VCORE EDC MAC 125A

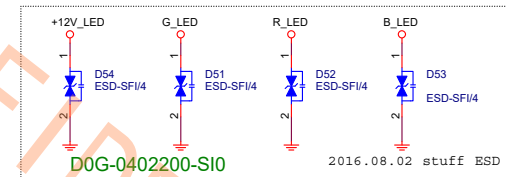
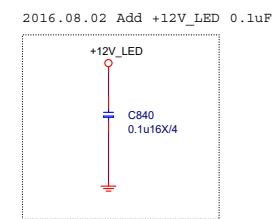
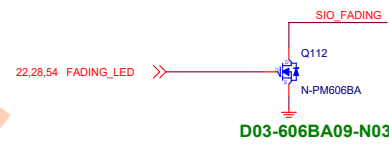
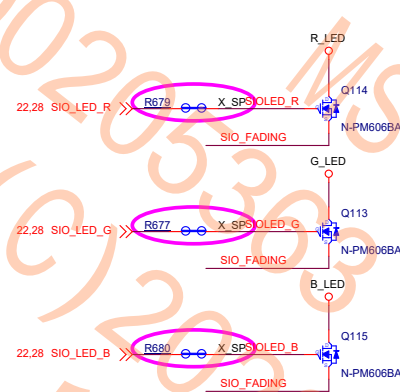
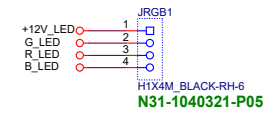
NB EDC MAX75A

RT9553 PIN5: When start OV/UV, RESET delay time can meet SPEC 15us.



CPU POWER CONNECTOR



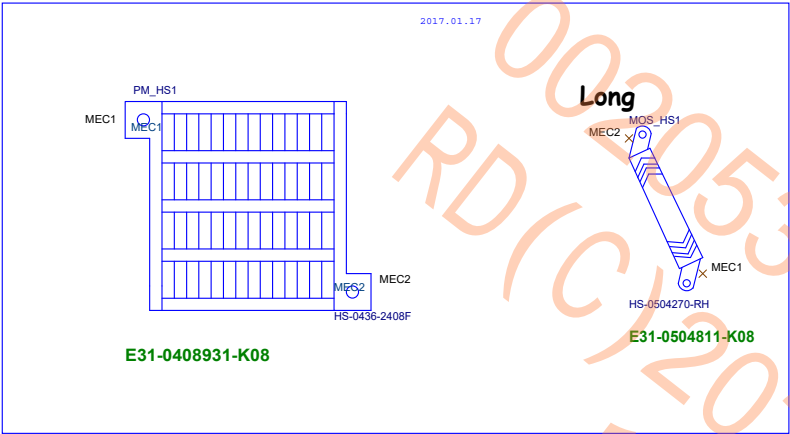


FCH LED Place under Heat-sink

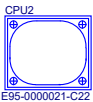
2016.11.25

LED
紅 : DOC-040S600-E07
白 : DOC-040S300-E07

HEAT SINK

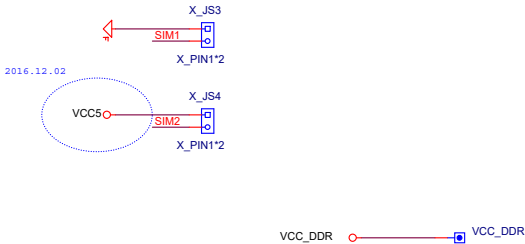


CPU Socket



RETENTION MODULE
E95-0000022-C22

Simulation



MANUAL PART

UEFI1
G51-M1SPXXA-A09
G51-M1SPXXA-A09

MKT1
G51-M1SPPP35-Q13
G51-M1SPPP35-Q13

cFosSoftware
X_Y02-MU00170-CFO
Y02-MU00170-CFO

BATI_X1
BATI-SOCR2032-RH
D06-0100101-P01

路祥雅
HDMI_LA1
Label
HDMI
HDMI LABEL
Y01-RHDMI03-000



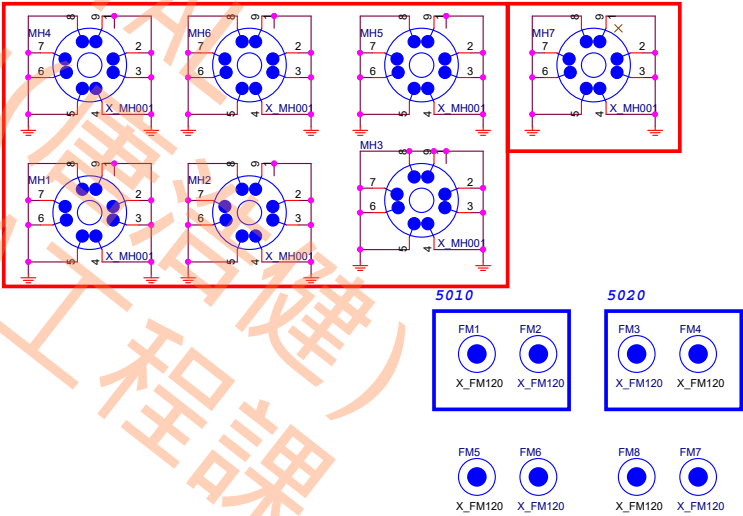
XSPLIT_LA1
Label
HDMI
X_SPLIT LABEL
Y02-MA00401-XSP

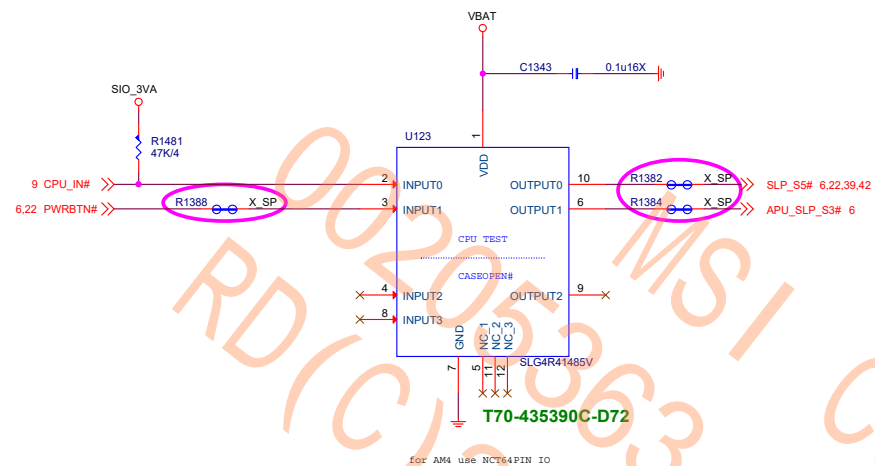
SSE_LA1
Label
HDMI
X_SSE LABEL
Y02-MA00101-SSE

REF1
OPT
X_FCH

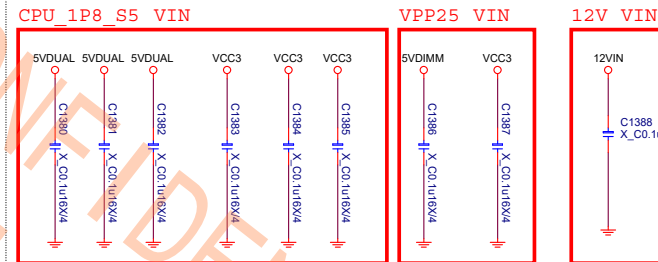
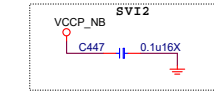
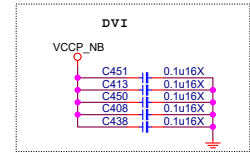
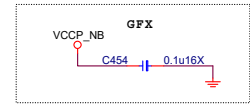
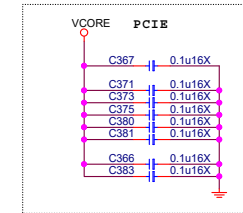
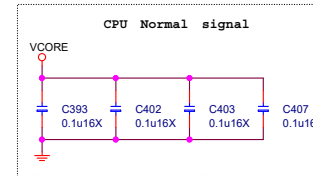
REF2
OPT
X_MKT

Optics Orientation Holes





Moat Cap



RTC & Clear CMOS Circuit

